# 1st Korea HEP-FPGA Firmware Developers' Forum 2025

## Thursday, 28 August 2025

**Day 4: FPGA Timing & High-Speed Communication (09:00 - 13:50)**

| time | [id] title | presenter |
|---|---|---|
| 09:00 | [14] Clock Management and Timing Closure in FPGA | |
| 09:45 | [15] High-Speed Serial Links (1) | |
| 10:30 | Coffee Break | |
| 10:45 | [16] High-Speed Serial Links (2) | |
| 11:30 | Lunch and end of Forum | |