Introduction to FPGA boards, handling clocks, programming FPGAs, Pynq-Z2 board

What does a FPGA have?

Each FPGA has a link for information

Table 1: **Summary of Spartan-3 FPGA Attributes**

Device	System Gates	Equivalent Logic Cells(1)	CLB Array (One CLB = Four Slices)			Distributed RAM Bits (K=1024)	Block RAM Bits (K=1024)	Dedicated Multipliers	DCMs	Max. User I/O	Maximum Differential I/O Pairs
			Rows	Columns	Total CLBs						
XC3S400(2)	400K	8,064	32	28	896	56K	288K	16	4	264	116

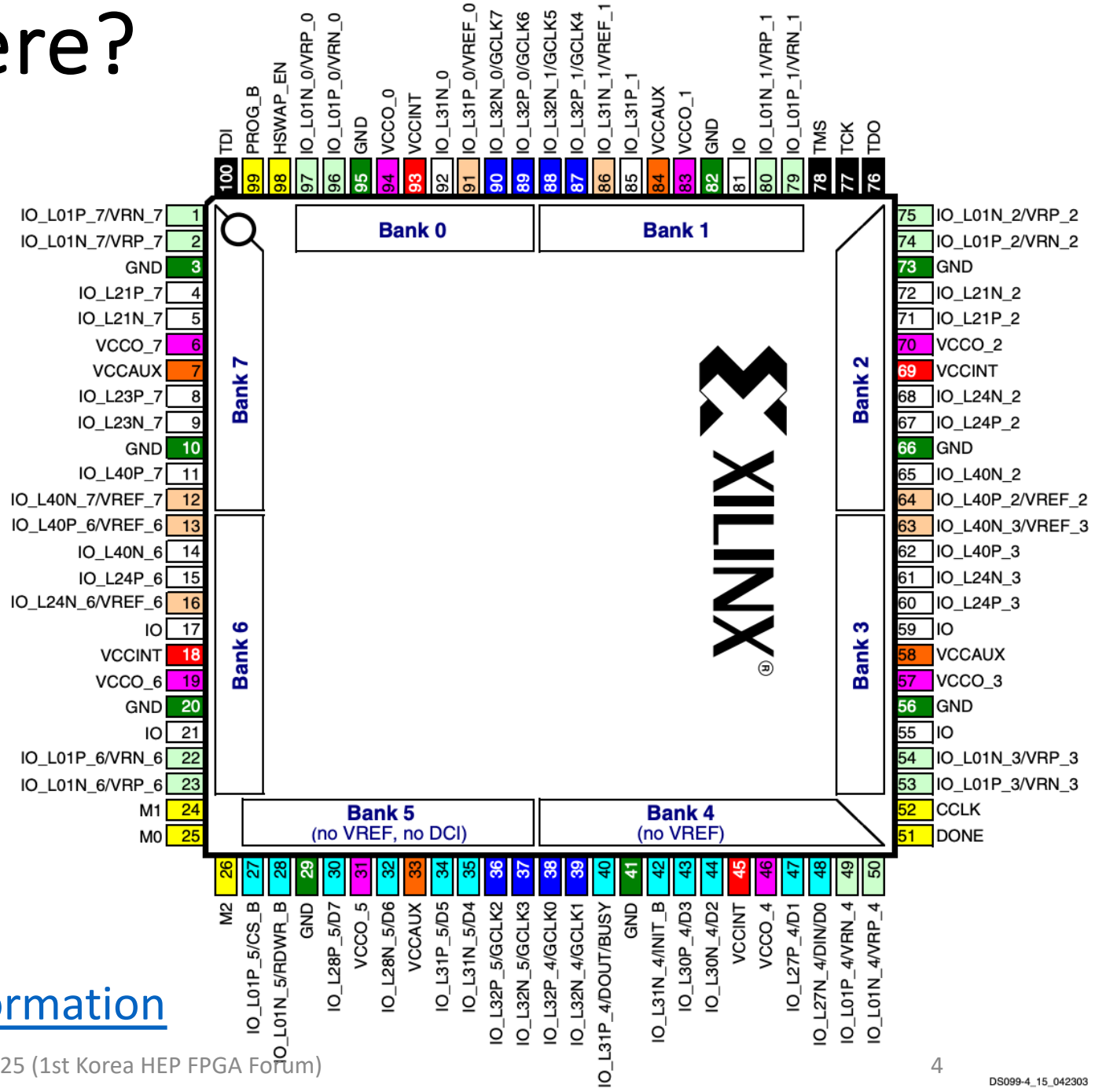
- CLB (Configurable Logic Block): SliceLUTs, Flip-flops
- BRAM (Block RAM): Memory for logic
- Multipliers: Multiplication components
- Digital Clock Manager (DCM): Modifies clk. Doesn't generate clk.
- Input/Output (I/O) interface pins: Pins logic is connected to

What do we need to provide to FPGAs?

- Power: FPGA needs power to work.
- Clock: Clock is needed for flip-flops.
- FPGA configuration method:
  - FPGA configuration is erased when power turns off.
  - Need to provide configuration to FPGA after turning on.
  - Two general methods: Using external memory chip; Another device (ex: computer) sends configuration (via JTAG protocol)

What FPGA pins are there?

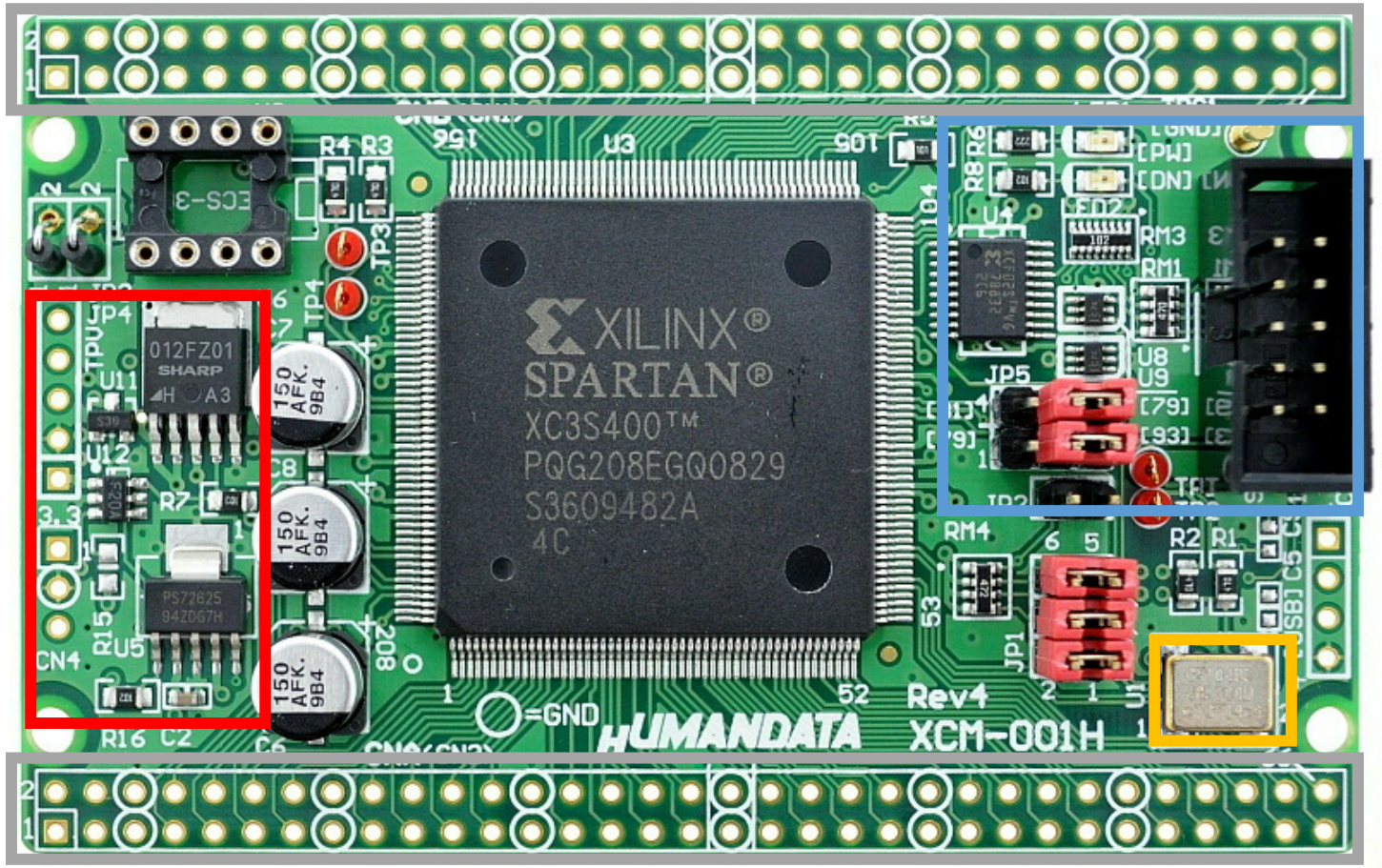
22	**I/O:** Unrestricted, general-purpose user I/O
14	**DCI:** User I/O or reference resistor input for bank
7	**CONFIG:** Dedicated configuration pins
0	**N.C.:** No unconnected pins in this package
12	**DUAL:** Configuration pin, then possible user I/O
8	**GCLK:** User I/O or global clock buffer input
4	**JTAG:** Dedicated JTAG port pins
10	**GND:** Ground
7	**VREF:** User I/O or input voltage reference for bank
8	**VCCO:** Output voltage supply for bank
4	**VCCINT:** Internal core voltage supply (+1.2V)
4	**VCCAUX:** Auxiliary voltage supply (+2.5V)



[Link for FPGA information]

Boards that have FPGAs

- Board supports FPGA
  - Power
  - Clock
  - Memory/Programming
  - Connectors for I/O
- How do I know this?



Simple FPGA board. [Board ref]

Board schematic tells what is connected to what

[Link to schematic]

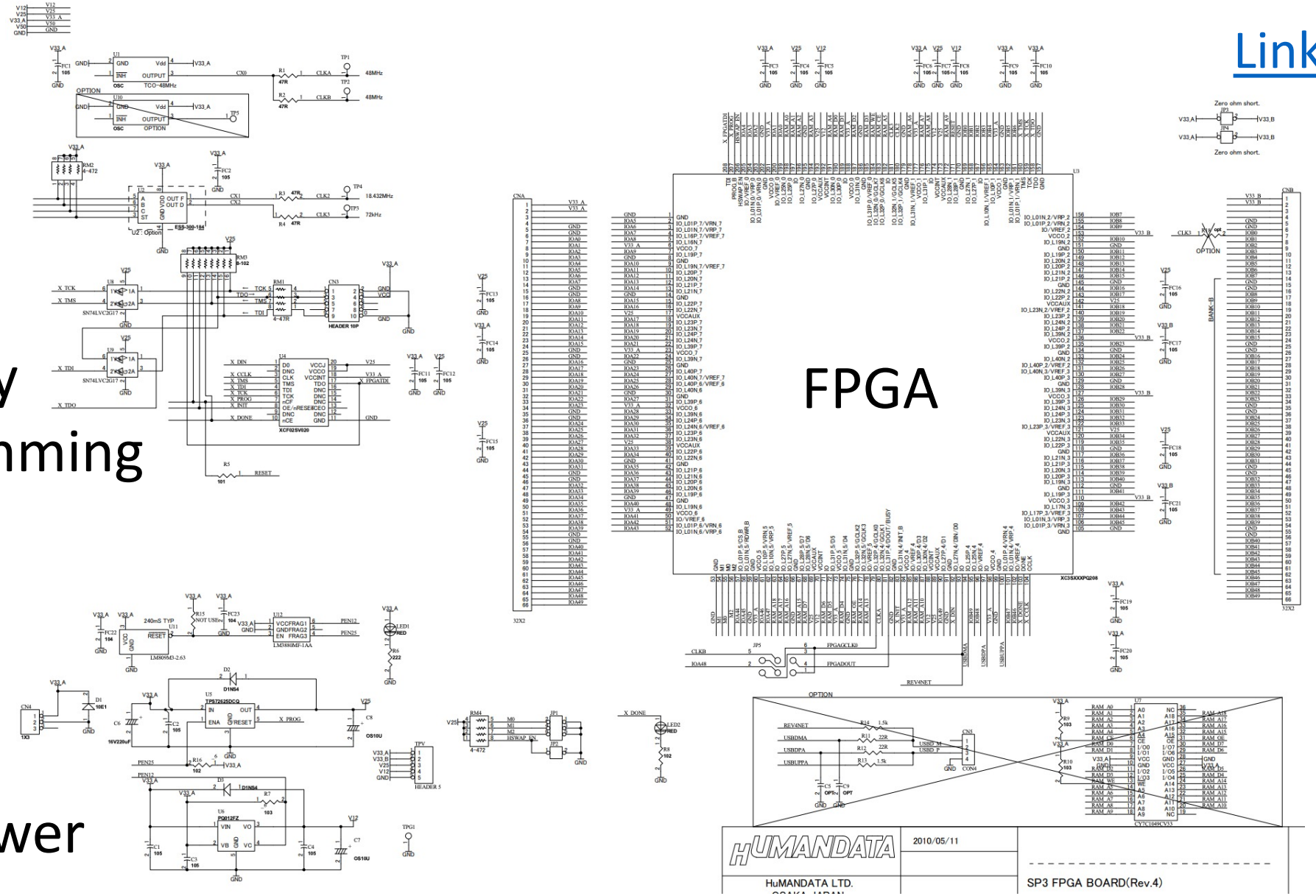
Clock

Memory Programming

FPGA

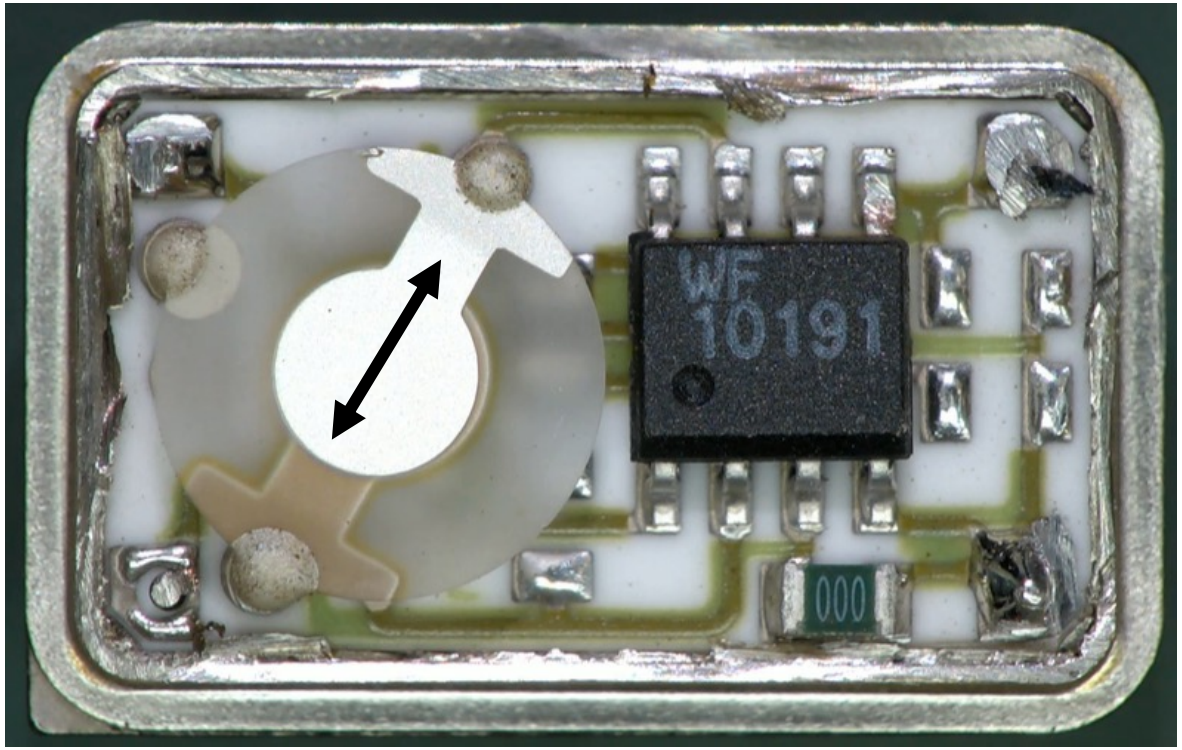
Connector

Power

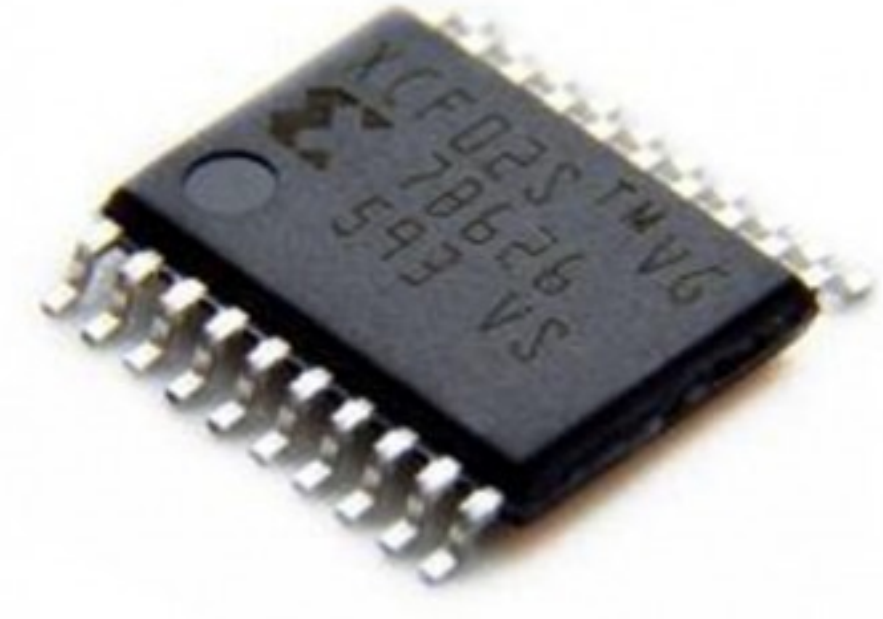


Clocks are generated with electric oscillators

- A crystal of piezoelectric material vibrating at resonance can be used to create a clock with precise frequency.



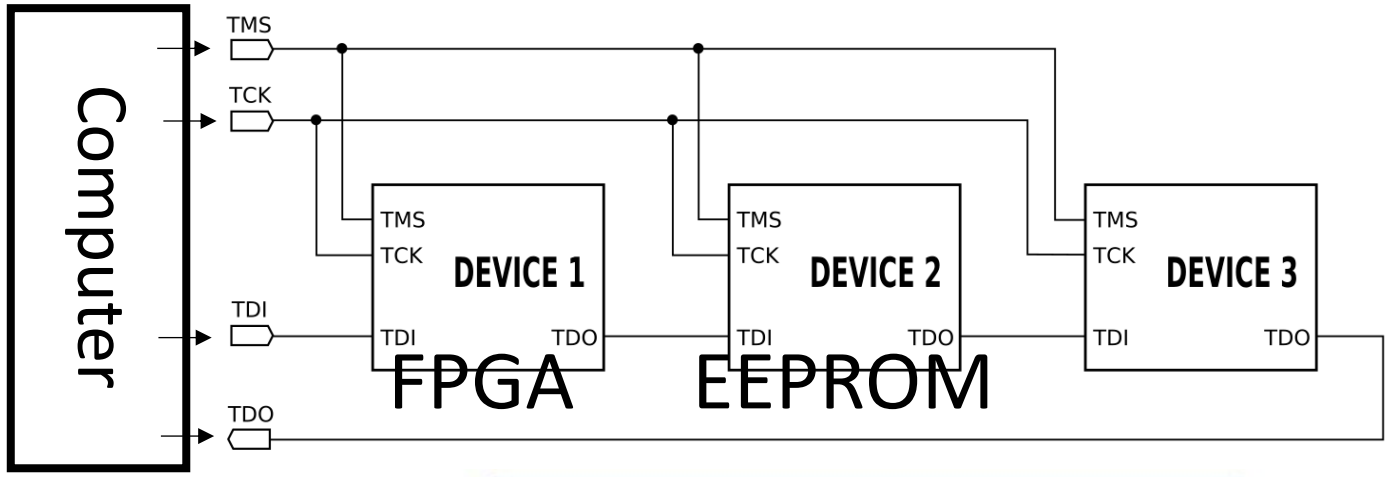
Memory using EEPROM

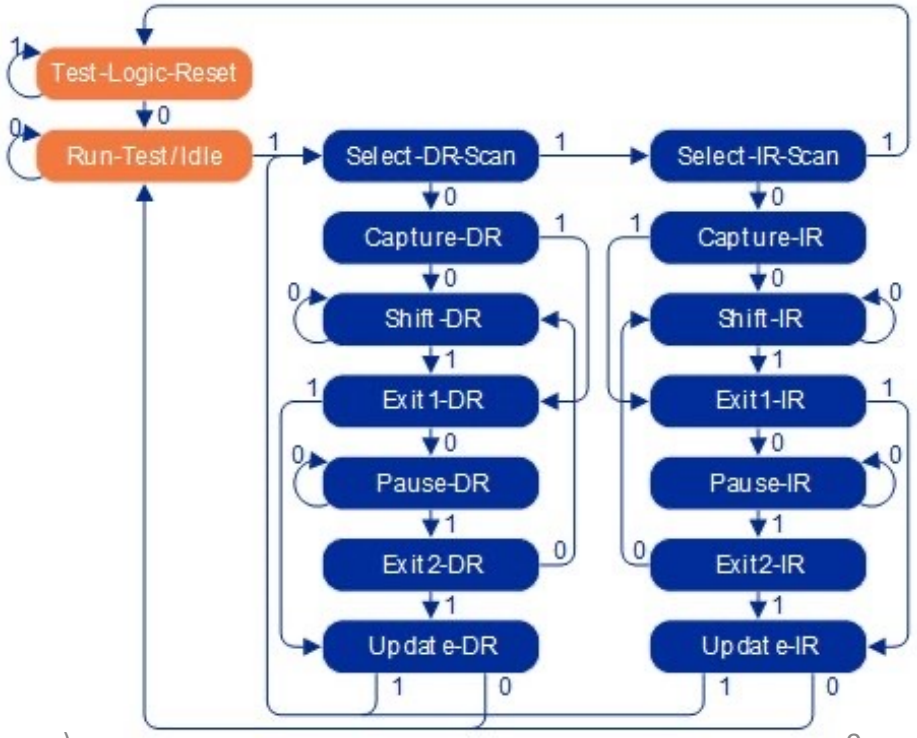


- EEPROM: Electrically erasable programmable read-only memory.
  - Normally read-only.
  - But can erase and program, if needed.
- Retains data, even after power off.
- Provides configuration data to FPGA after power on board.
- FPGA can be used to program the EEPROM!

JTAG protocol used for programming FPGA

- A communication protocol.
- Requires 4 wires (pins)
  - ➢TCK: clock
  - ➢TMS: mode select
  - ➢TDI: data input
  - ➢TDO: data output
- Can program FPGA and also EEPROM





To be able to use a FPGA

1. Need to know how to connect logic to FPGA pins.

   - Each FPGA have different pins.

     AMD/Xilinx
   - FPGA manufacture provides datasheets about FPGA pins.

2. Need to know how FPGA pins are connected on board.

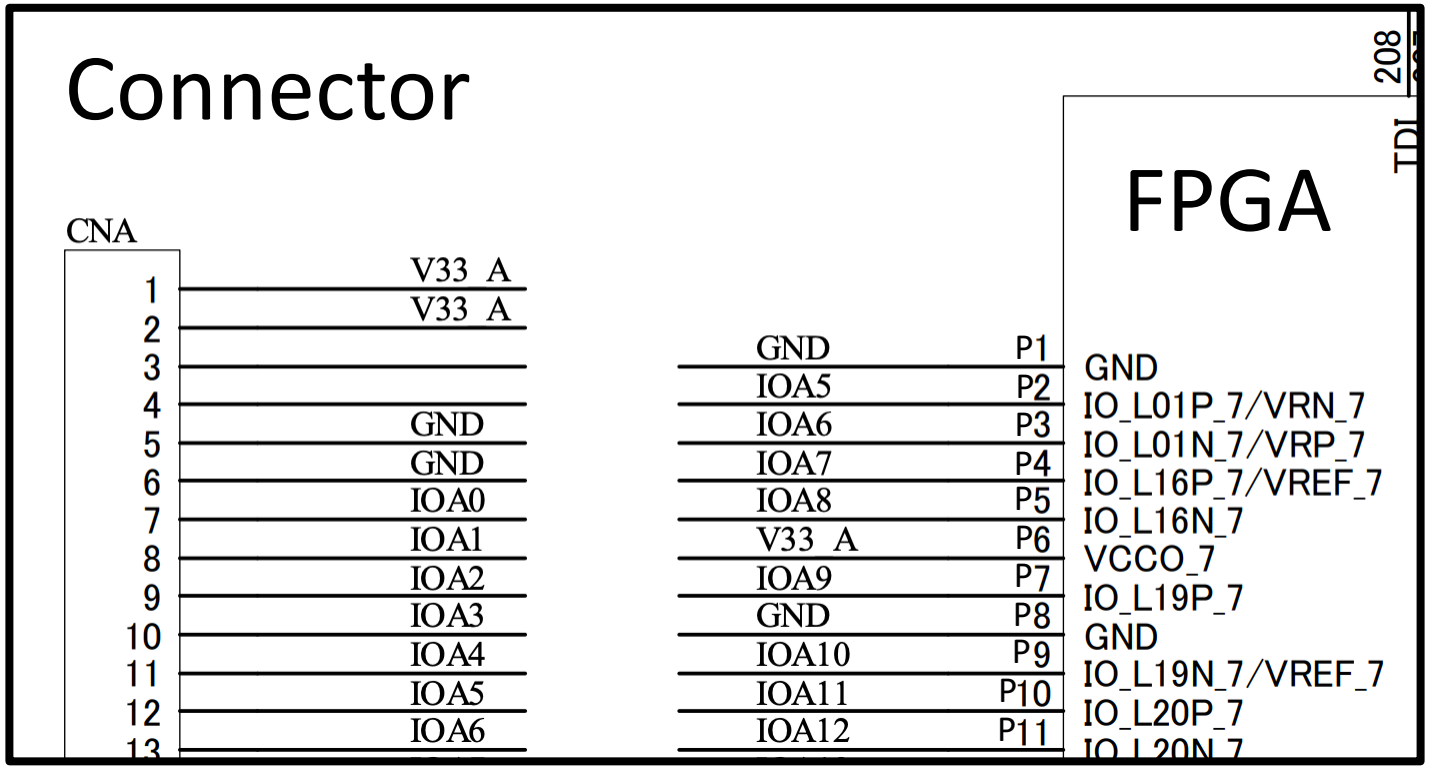
   - Board developer/manufacture provides information on how FPGA pins are connected.

How are the board connectors linked to FPGA pins?

- Look at board schematic

- Connector 12 is connected to IOA5.

- IOA5 is connected to IO_L01P_7/VRN_7 (Pin: P2)



How to connect logic to FPGA pins?

- AMD provides "pin number" that can be used to connect to logic.

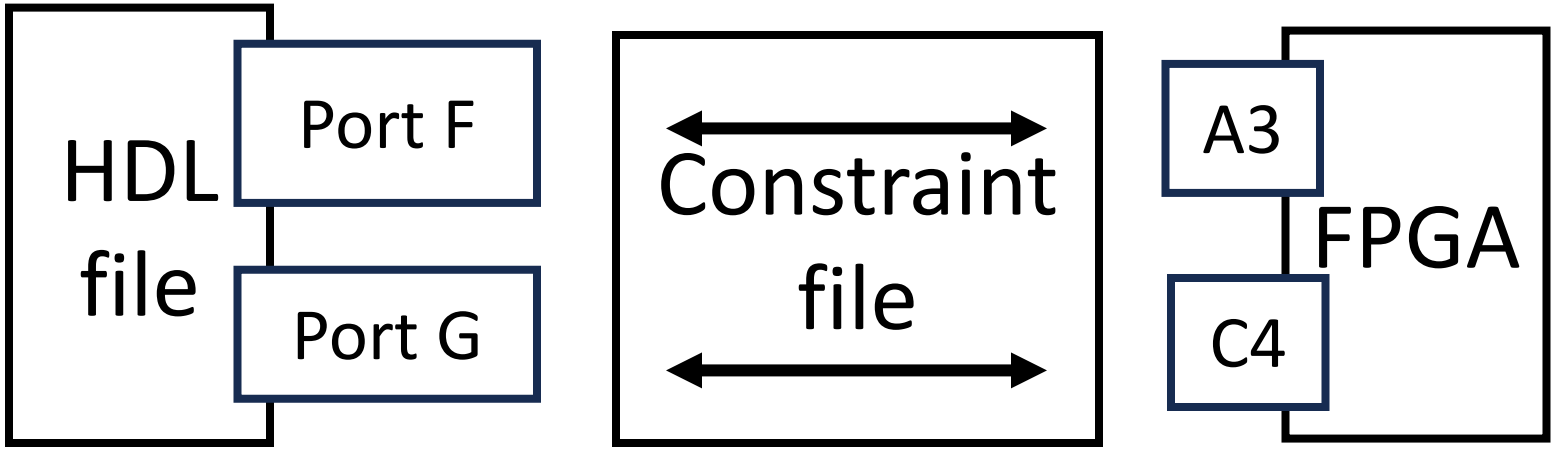


Table 89: **CP132 Package Pinout**

Bank	XC3S50 Pin Name	CP132 Ball	Type
0	IO_L01N_0/VRP_0	A3	DCI
0	IO_L01P_0/VRN_0	C4	DCI
0	IO_L27N_0	C5	I/O
0	IO_L27P_0	B5	I/O
0	IO_L30N_0	B6	I/O
0	IO_L30P_0	A6	I/O
0	IO_L31N_0	C7	I/O
0	IO_L31P_0/VREF_0	B7	VREF
0	IO_L32N_0/GCLK7	A7	GCLK
0	IO_L32P_0/GCLK6	C8	GCLK

- Write constraint file to connect HDL ports to FPGA pins.

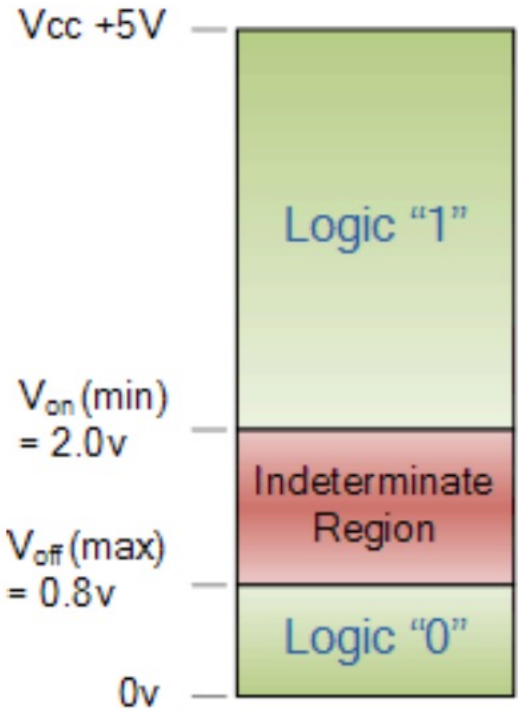
```
set_property -dict { PACKAGE_PIN A3   IOSTANDARD LVCMOS18 } [get_ports F]
```

Digital logic voltage levels and FPGA I/O pins

- What is the voltage of digital logic 1?
  - Depends on the ”standard” of digital logic.

Standard	Logic 0	Logic 1
TTL	0 to 0.8 Volts	2.0 to 5.0 Volts
CMOS	0 to 1.5 Volts	3.0 to 1.8 Volts

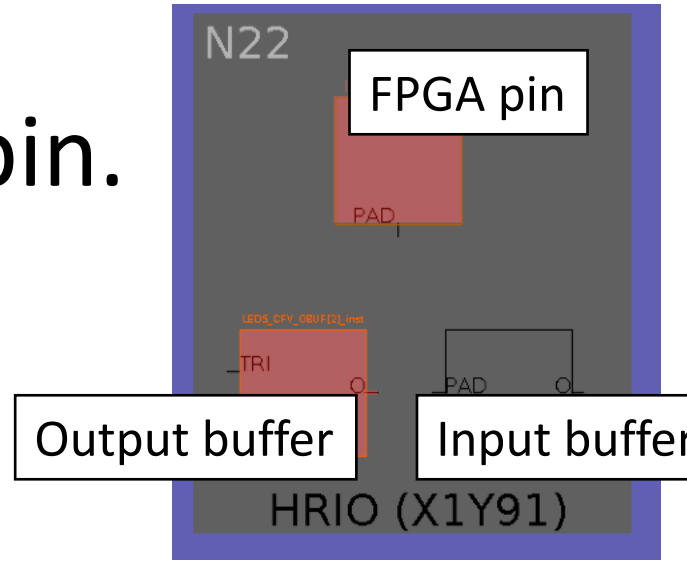
TTL standard



- FPGA pins are flexible.
  - Can set them to use/be different standards.

Digital logic voltage levels and FPGA I/O pins

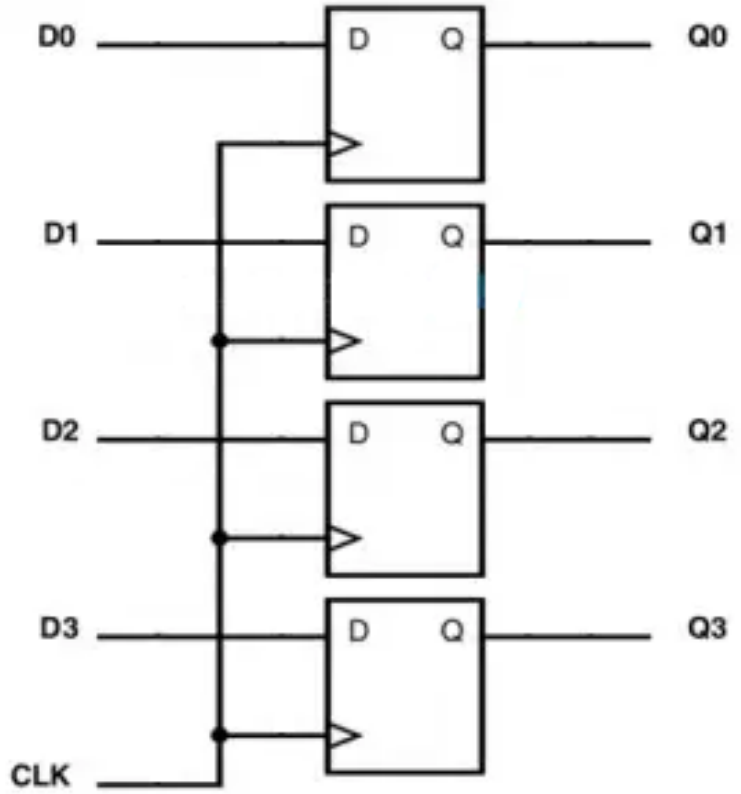
- FPGA pins can connect to Input / Output buffers.
- Buffers can be set to use different voltages/standards.
- Use the constraint file to set standard of pin.
  - ➢ Vivado will set buffer voltage accordingly.




```
set_property -dict { PACKAGE_PIN A3   IOSTANDARD LVCMOS18 } [get_ports F]
```

FPGA clock pins

- The FPGA clock pin is special.
  - Synchronous logic uses many flip-flops.
  - Clock has to connect to many flop-flops.
  - There is a special switch matrix that is connected to many components.



Global Clock Lines

In each 7 series FPGA (except XC7S6 and XC7S15), 32 global clock lines have the highest fanout and can reach every flip-flop clock, clock enable, and set/reset, as well as many logic inputs. There are 12 global clock lines within any clock region

From AMD datasheet

FPGA clock pins

- Only certain FPGA pins are connected to Global Clock Line.
- Check schematic to find what frequency clock connected.

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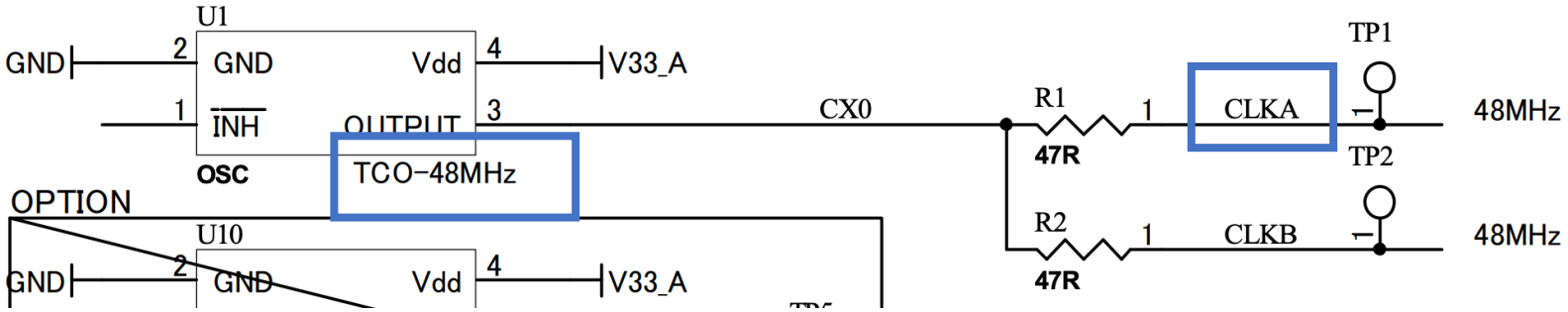
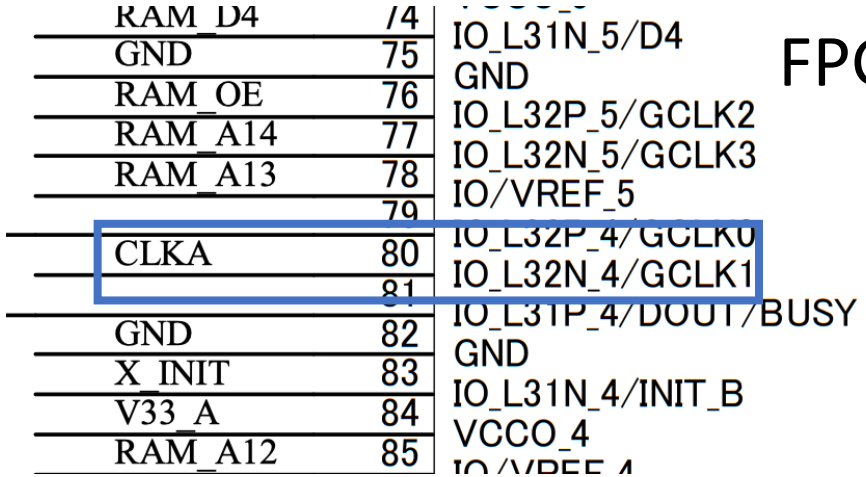
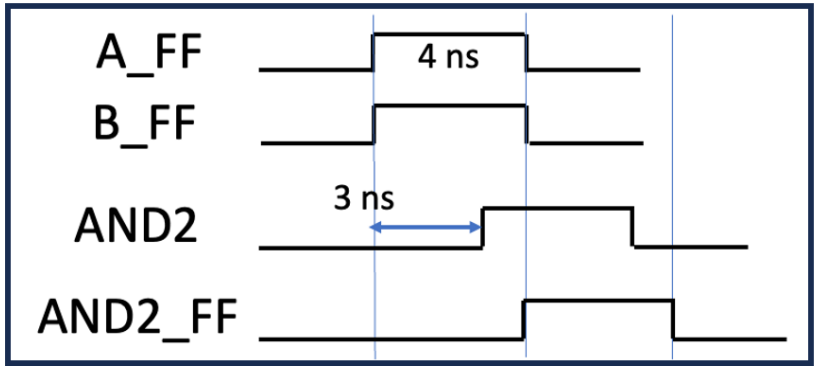
0	IO_L27P_0	B5	I/O
0	IO_L30N_0	B6	I/O
0	IO_L30P_0	A6	I/O
0	IO_L31N_0	C7	I/O
0	IO_L31P_0/VREF_0	B7	VREF
0	IO_L32N_0/GCLK7	A7	GCLK
0	IO_L32P_0/GCLK6	C8	GCLK





FPGA

How to handle clock pins in code?



- We'll use Vivado to synthesize HDL.
- Vivado needs to tell us if synchronized logic can work with clock frequency.
  - Is 4ns long enough for AND2?
- Constraint file is used to tell Vivado clock frequency

```
create_clock -name clkin_group -period 20.833 [get_ports clkin]
```

Nanoseconds = 48 Mhz

How to handle clock pins in code?

- We also need to tell Vivado to use the global clock line.
  - Because pins (Ex: A7) can be used as clock pin and also as normal I/O.

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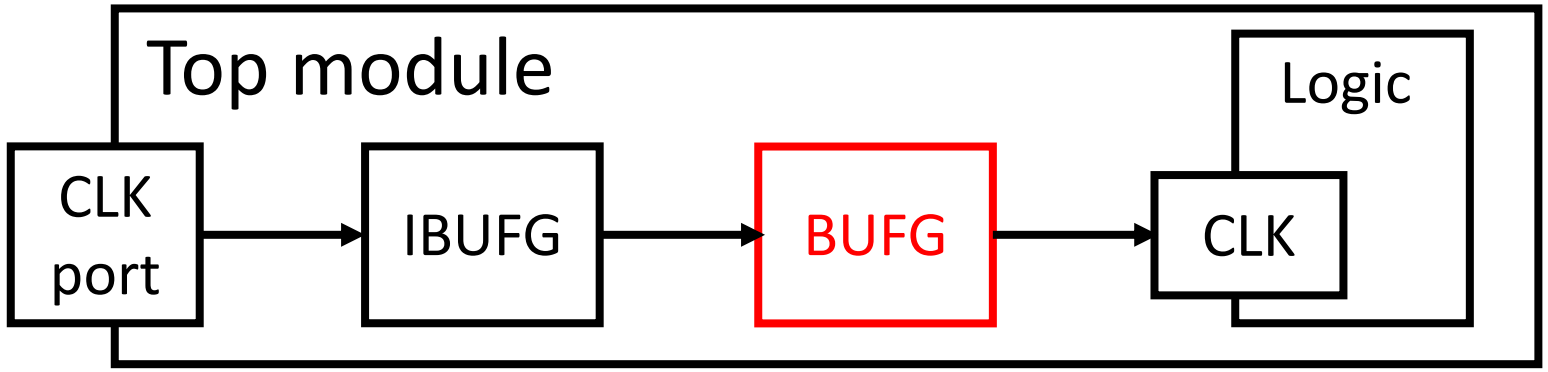
0	IO_L27P_0	B5	I/O
0	IO_L30N_0	B6	I/O
0	IO_L30P_0	A6	I/O
0	IO_L31N_0	C7	I/O
0	IO_L31P_0/VREF_0	B7	VREF
0	IO_L32N_0/GCLK7	A7	GCLK
0	IO_L32P_0/GCLK6	C8	GCLK

- This can be done with below module structure in HDL.



How are FPGA are programmed?

- FPGAs can be programmed via JTAG or EEPROM.
- For quick testing, normally use JTAG. Takes few seconds.
  - ➢Computer write configuration data (firmware) to FPGA.
- For more permanent option, EEPROM are used. Done in steps.
  1. Erase EEPROM and write firmware to EEPROM. Takes many minutes.
  2. Turn off board power. This erases configuration on FPGA.
  3. Turn on board power. FPGA automatically reads from EEPROM.

FPGA manufacturers

- Xilinx → AMD: Well-known and well supported
- Altera → Intel: Well-known and well supported
- Microchip: Less support. But will be used in some CMS boards, due to radiation tolerant FPGA (Polarfire FPGA)
- Lattice : Less support

AMD FPGAs

- Spartan FPGA
- Artix FPGA
- Kintex FPGA
- Vertex FPGA

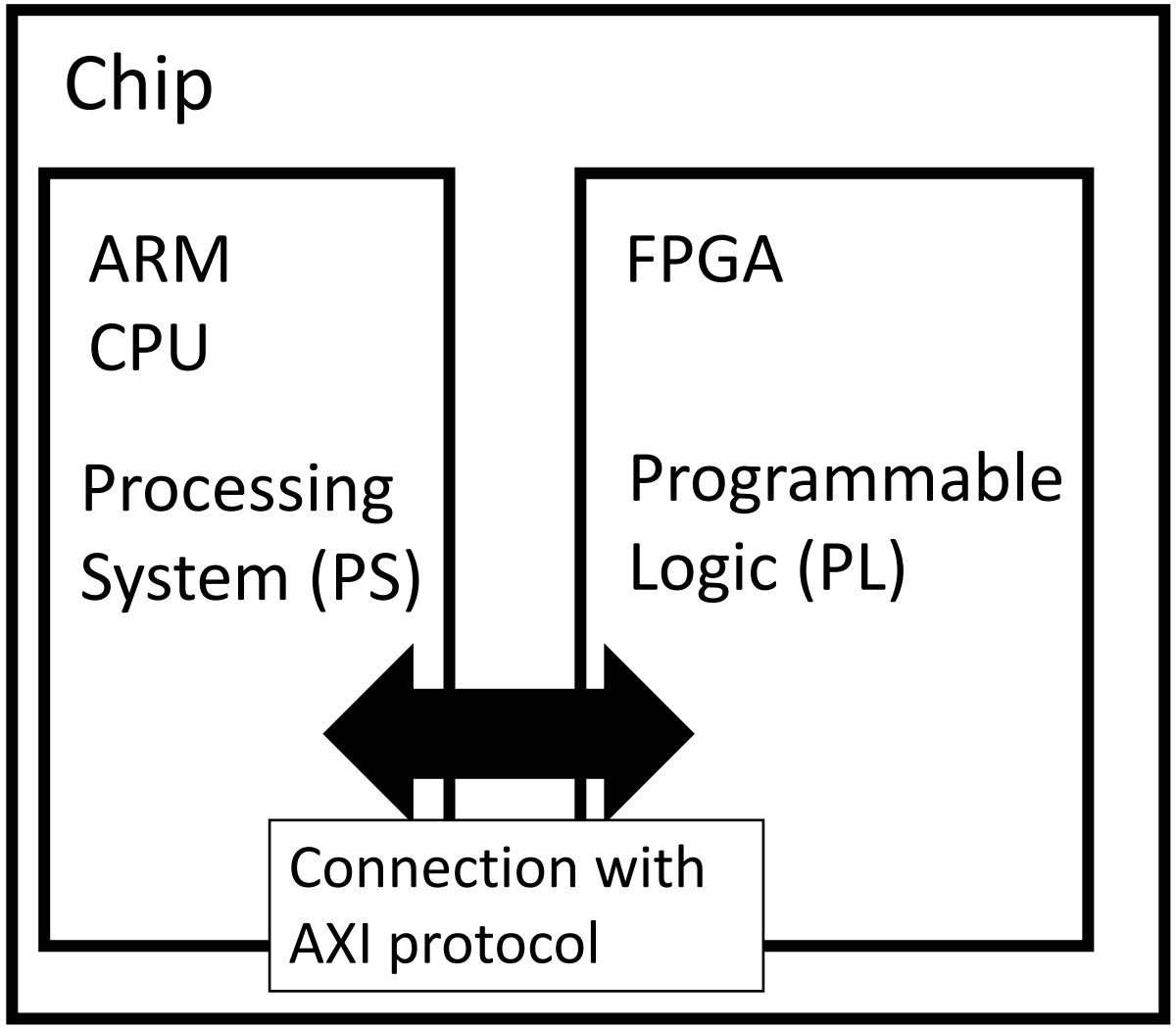
Generally cheaper
Less resources
Limited to slower clock

Generally expensive
More resources
Can use faster clock

- Each FPGAs also have “speed grade”. Determines how fast a clock one can use.
  - -1: Slow
  - -2: Middle
  - -3: Fastest

AMD Zynq FPGA

- FPGA combined with CPU
- FPGA and CPU can communicate through Advanced eXtensible Interface (AXI).

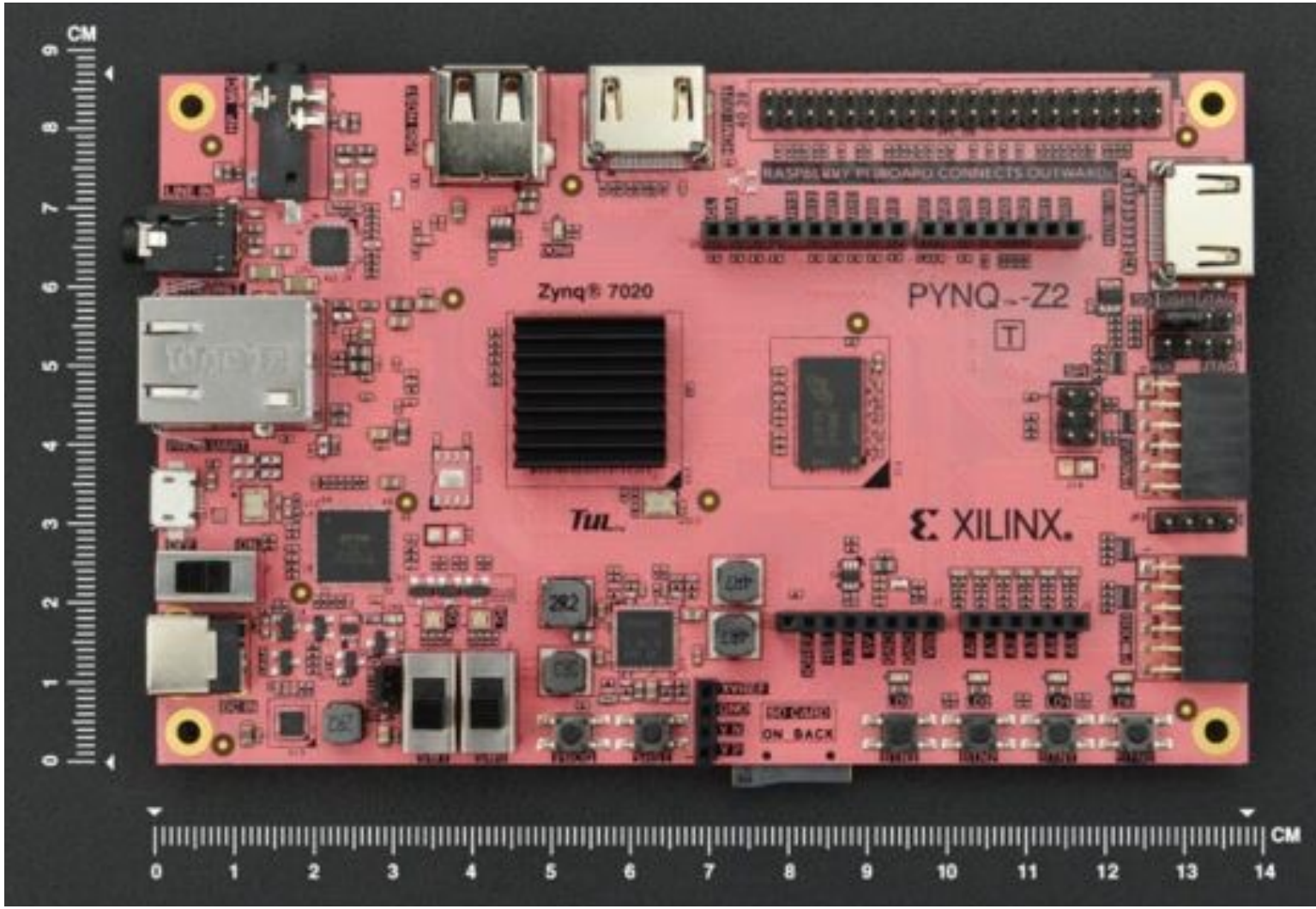


Pynq-Z2 board FPGA

- Board has Zynq

  XC7Z020-1CLG400C

  - 020: Zynq series type
  - -1: Speed grade
  - CLG: FPGA pin layout
  - 400 pins
  - C: Temperature limit



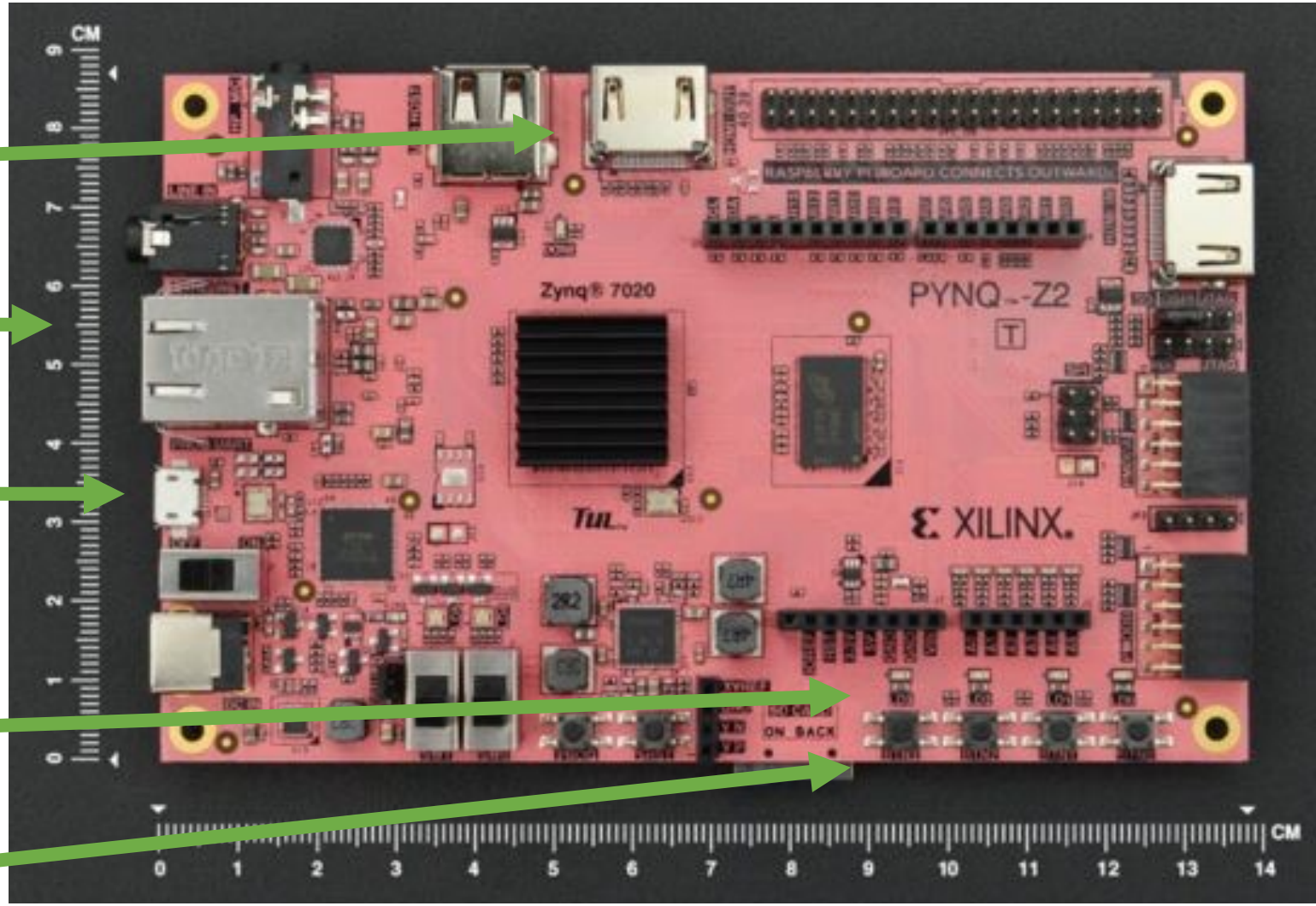
Resources of XC7Z020-1CLG400C

- Programmable logic cells, LUTs, Flip-flops are closely related.
  - ➢ Logic cell is just a marketing term
  - ➢ CLBs has LUT and FF included.
- BRAM: 140 × 36Kb
- DSP: 220

Device Name	Z-7020
Part Number	XC7Z020
Xilinx 7 Series Programmable Logic Equivalent	Artix-7 FPGA
Programmable Logic Cells	85K
Look-Up Tables (LUTs)	53,200
Flip-Flops	106,400
Block RAM (# 36 Kb Blocks)	4.9 Mb (140)
DSP Slices (18x25 MACCs)	220

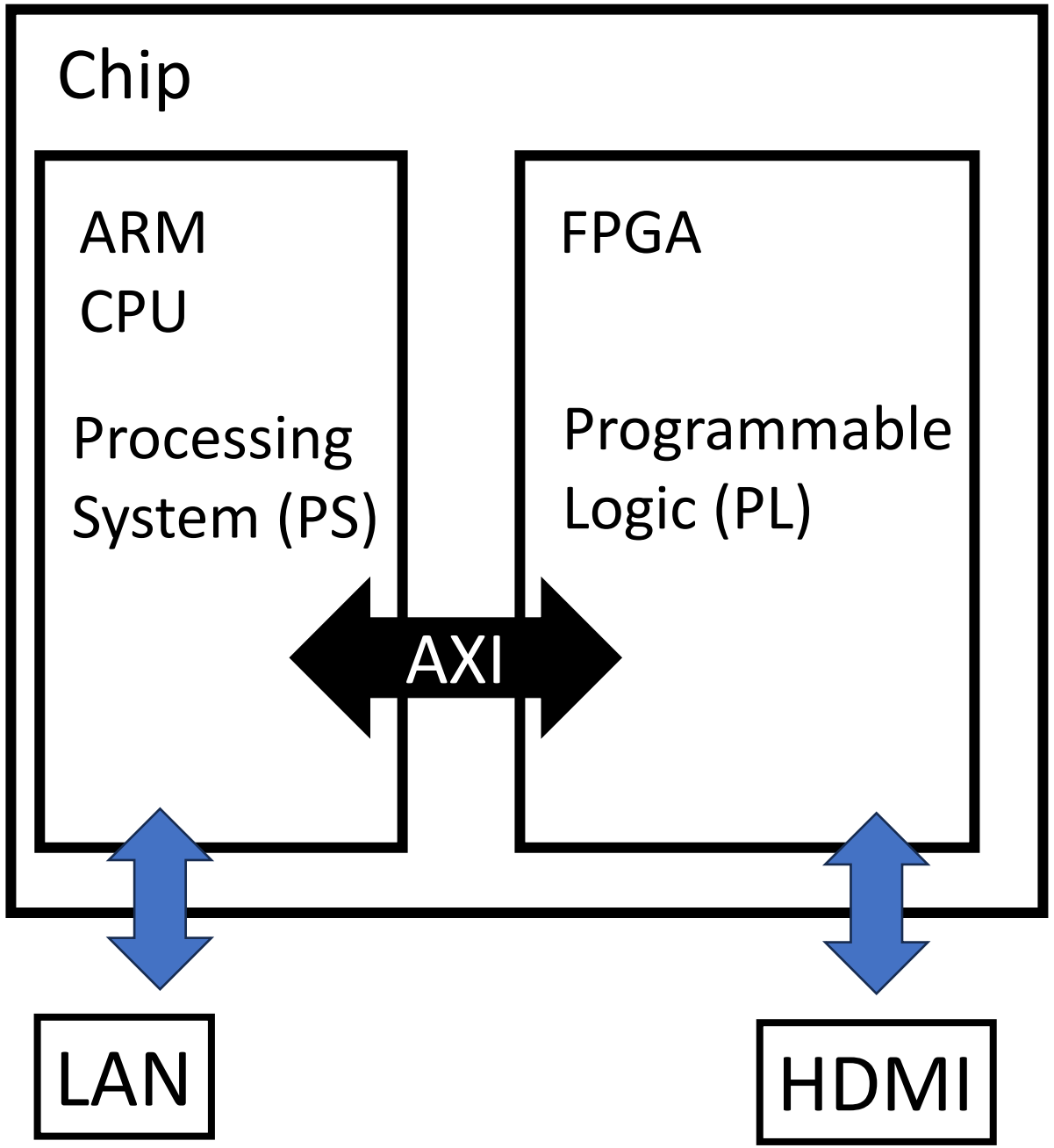
Pynq-Z2 board FPGA

- Board
  - HDMI port
  - LAN port
  - Programming / power port.
  - LEDs
  - Buttons



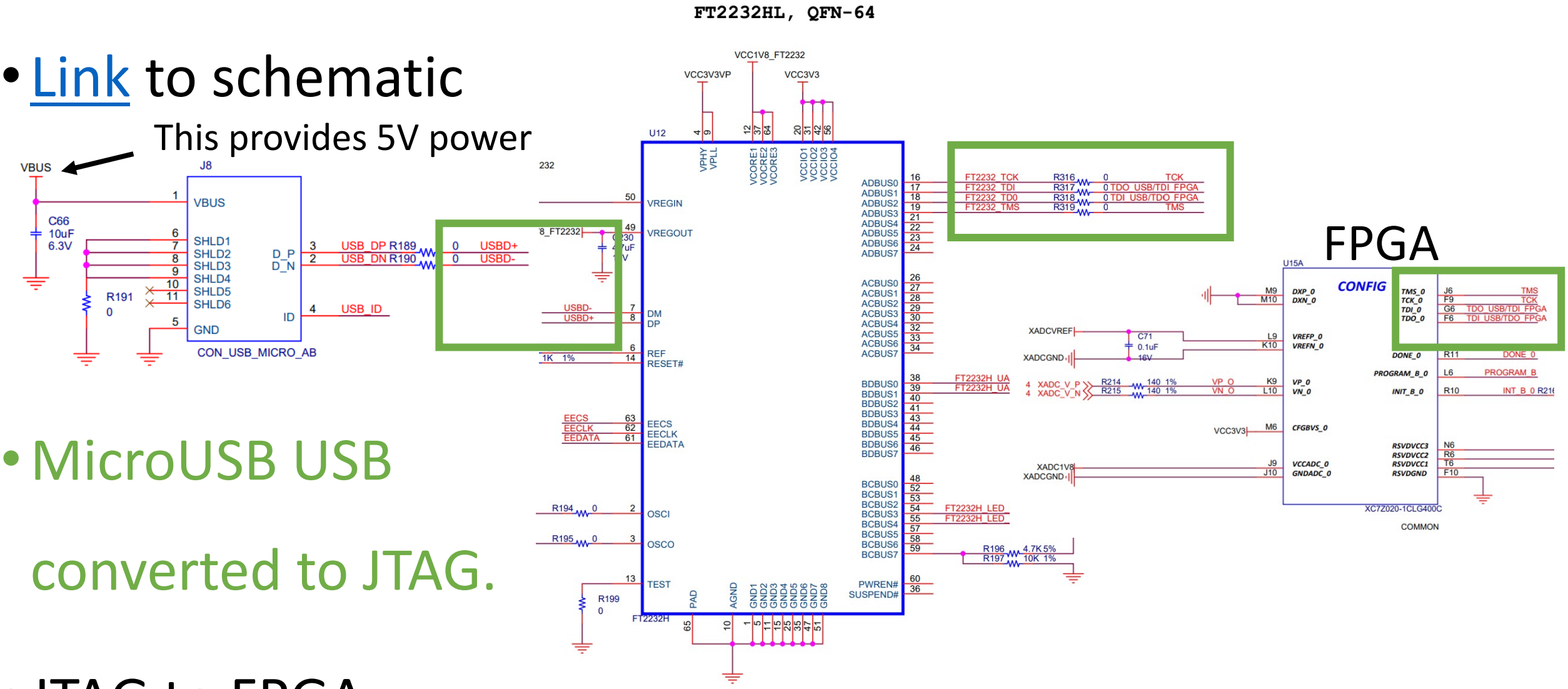
Pynq-Z2

- Some ports connected to CPU.
- Some ports connected to FPGA.
- We will only use FPGA (PL).



Pynq-Z2 schematic: How is FPGA programed?

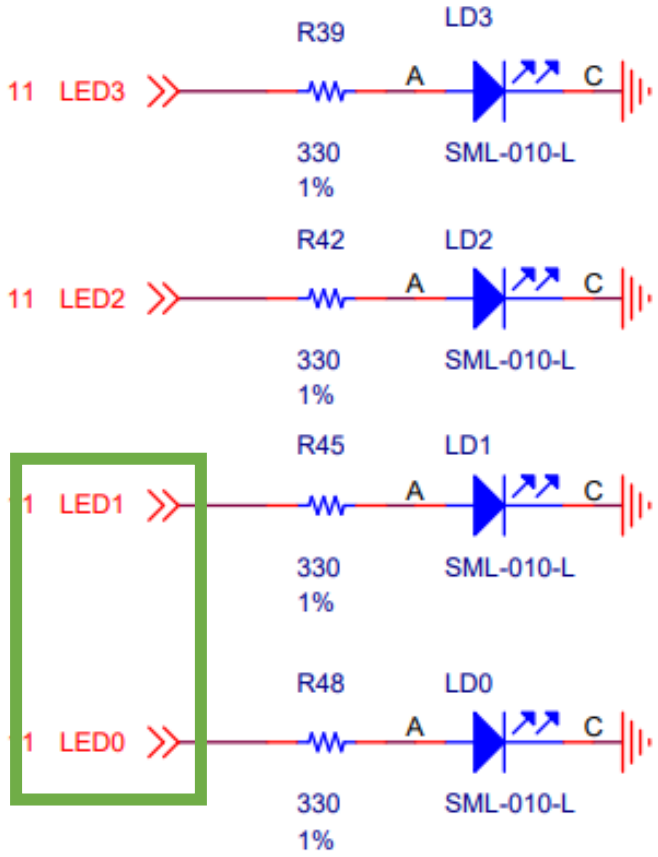
- Link to schematic

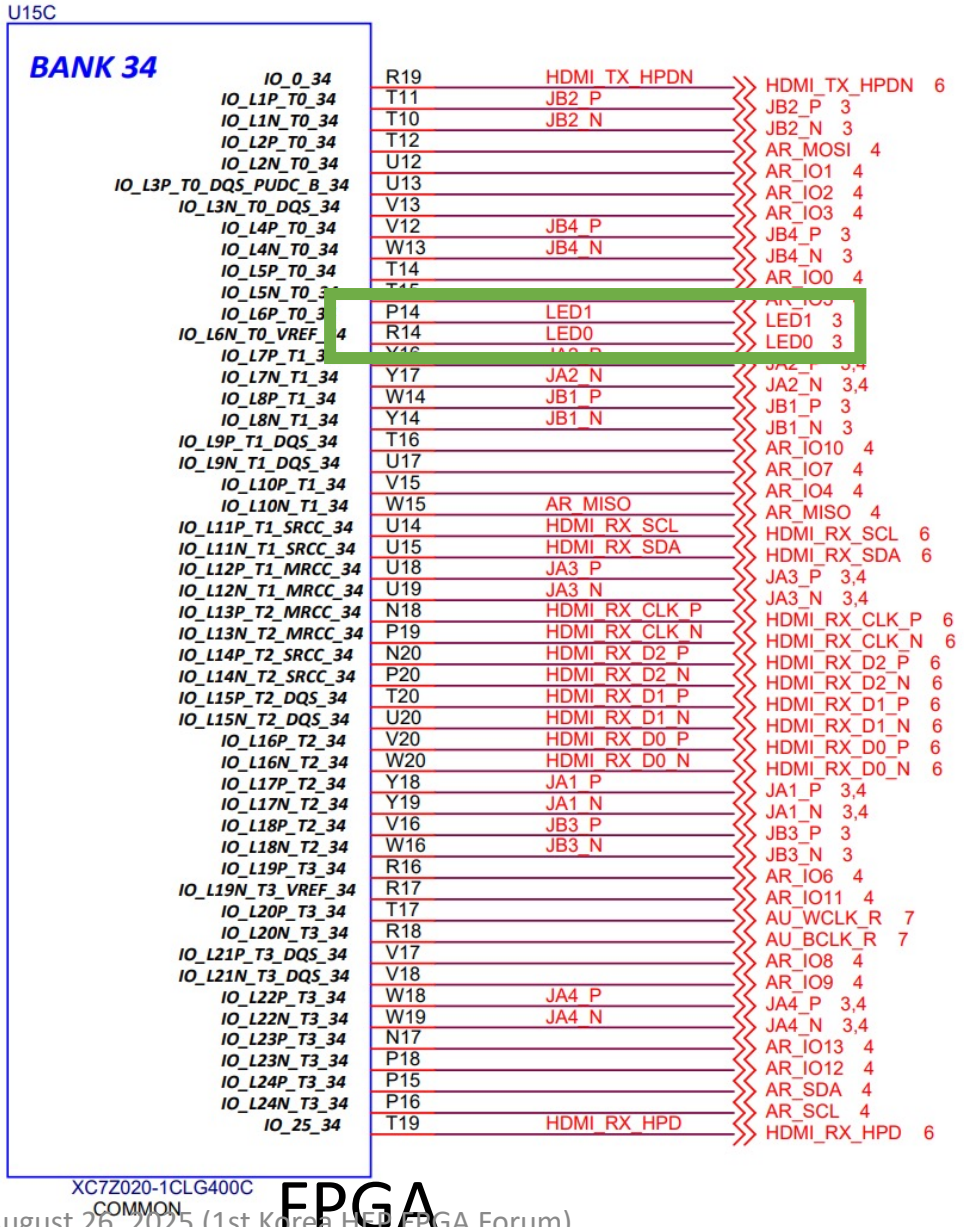


- MicroUSB USB converted to JTAG.
- JTAG to FPGA.

Pynq-Z2 schematic: What pin to use for LED?

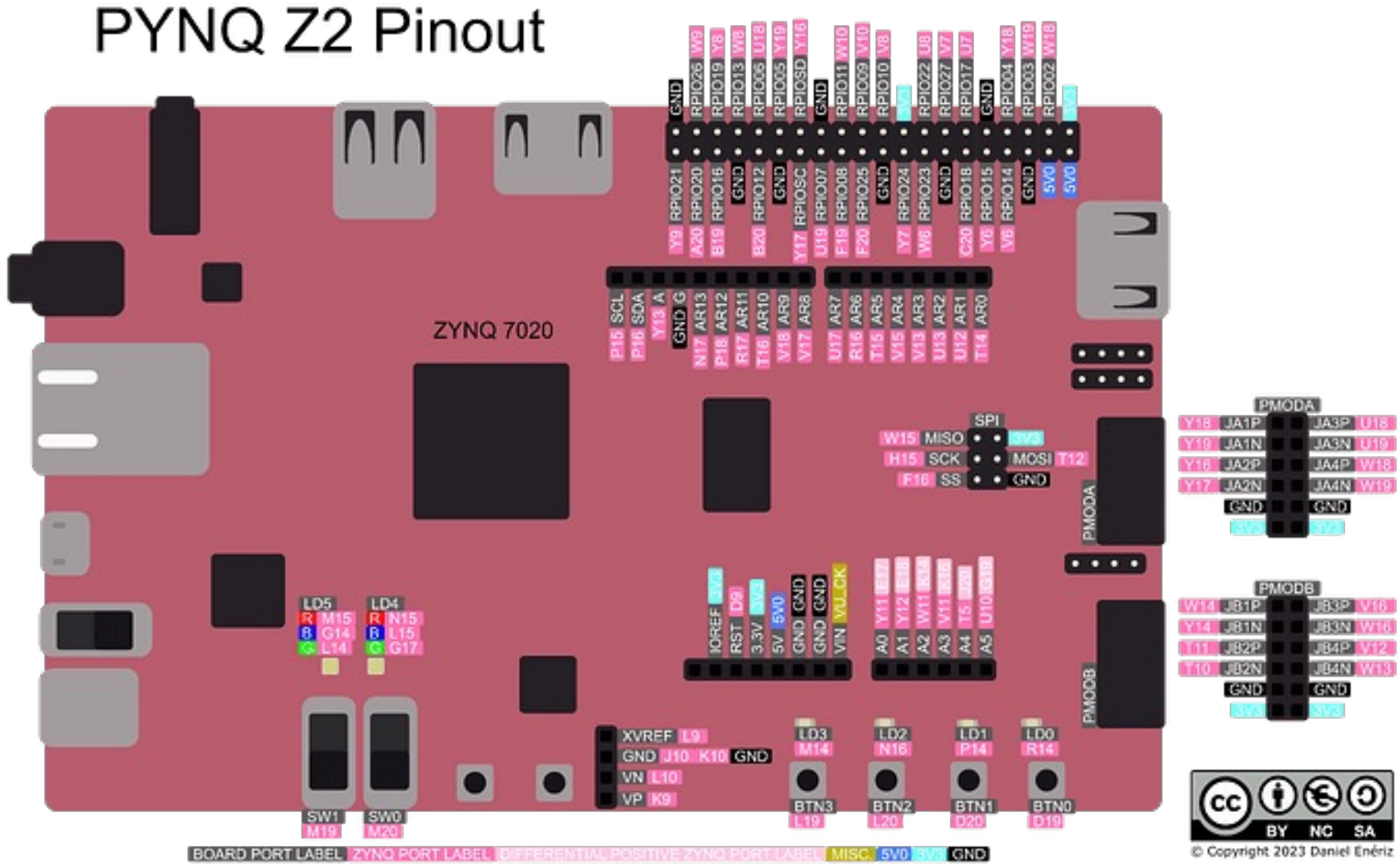
- Link to schematic





- LD0 is pin R14

Pretty image for FPGA pins: Link



Pynq-Z2 schematic: What clock can we use?

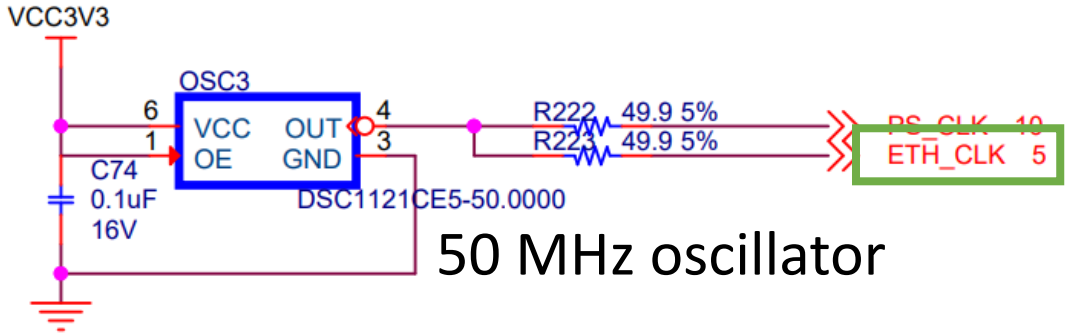
- Link to schematic
- 50 MHz oscillator goes to Realtek IC
- Realtek IC (125MHz) goes to FPGA (H16)

Realtek link

6.2. Clock

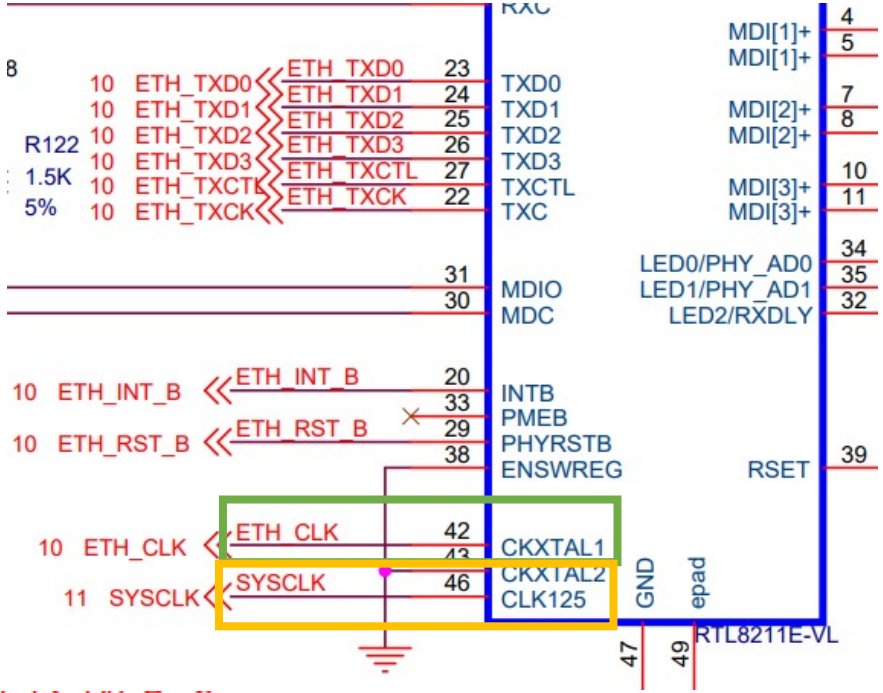
Table 2. Clock

Pin No. (48-pin)	Pin No. (64-pin)	Pin Name	Type	Description
42	61	CKXTAL1	I	25/50MHz Crystal Input. If a 25/50MHz oscillator is used, connect CKXTAL1 to the oscillator's output (see section 10.3, page 57 for clock source specifications).
43	62	CKXTAL2	O	25/50MHz Crystal Output. Connect to GND if an external 25/50MHz oscillator drives CKXTAL1.
46	1	CLK125	O/PD	125MHz Reference Clock Generated from Internal PLL. This pin should be kept floating if the 125MHz clock is not used by MAC.



50 MHz oscillator

FPGA



- How much did you understand? www.kahoot.it