FPGA in DAQ of Dual-Readout Calorimeter

EO Yun

On the behalf of Korea Dual-Readout Calorimeter team

1st Korea HEP-FPGA Firmware Developers' Forum 2025

2025 August 25

What did the Yonsei HEP?

- Dual-Readout Calorimeter
  - Fiber-based sampling calorimeter.
  - We get 2 kinds of readout channels : Scintillation and Cerenkov
    - Scintillation : all charged particle
    - Cerenkov : light particle (EM particle)
  - W/ dual-readout correction, the dual-readout calorimeter can get good hadronic energy resolution.

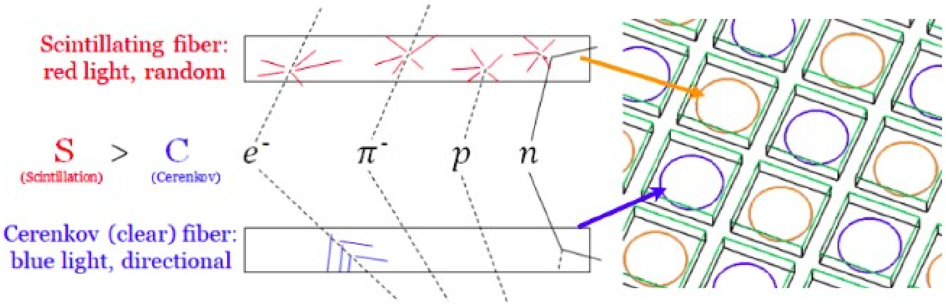
$$f_{em} = \frac{(h/e)_C - (C/S)(h/e)_S}{(C/S)[1-(h/e)_S] - [1-(h/e)_C]}$$

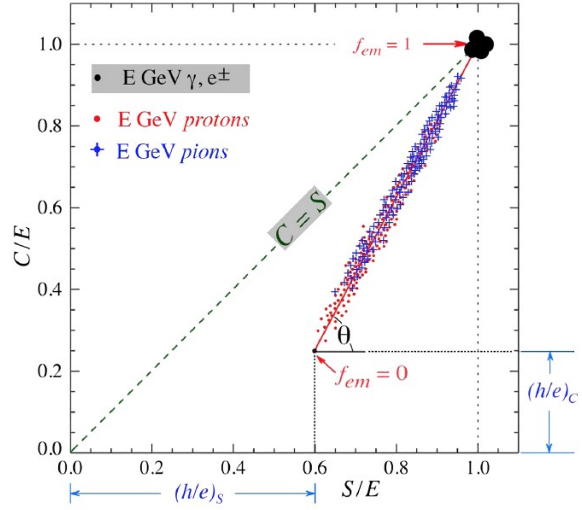
$$S/E = f_{em} + \frac{1-f_{em}}{(h/e)_S}$$

$$C/E = f_{em} + \frac{1-f_{em}}{(h/e)_C}$$

$$E = \frac{S - \chi C}{1-\chi}$$

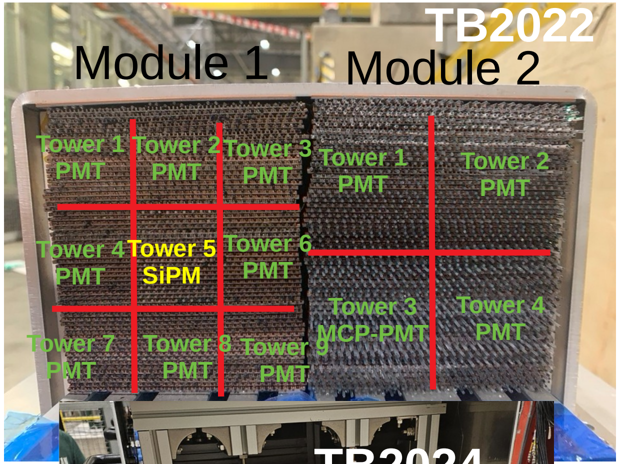
$$\theta = \cos^{-1}\left(\frac{1-(h/e)_S}{1-(h/e)_C}\right) = \cos^{-1}\chi$$

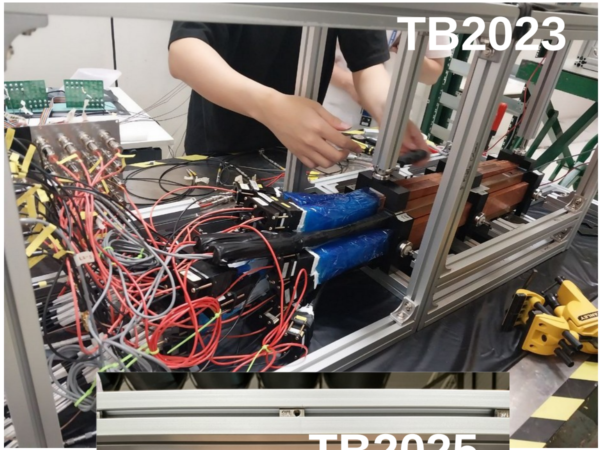


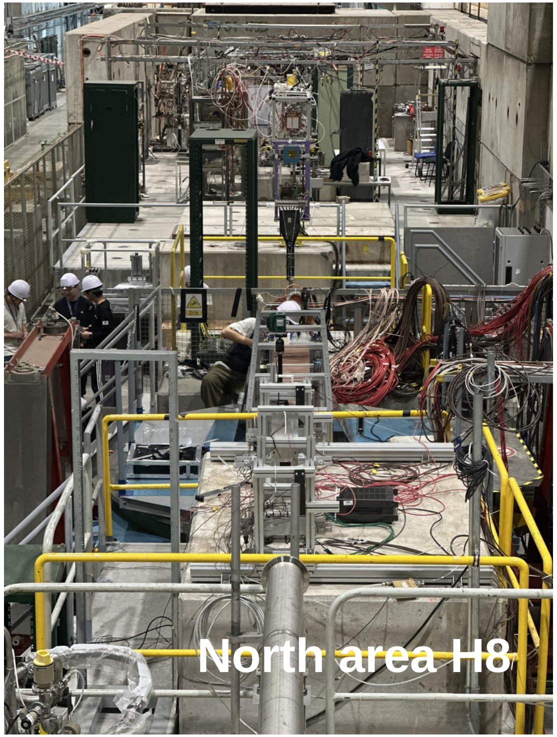


What did the Yonsei HEP?

- We conducted the testbeam on SPS and PS several years (2022 to 2025).

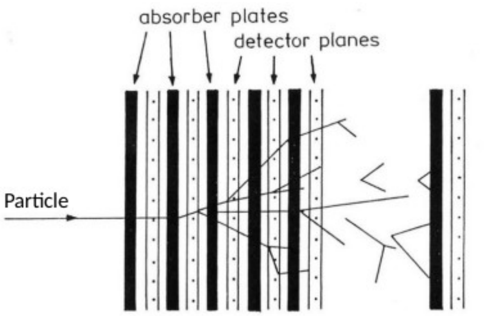




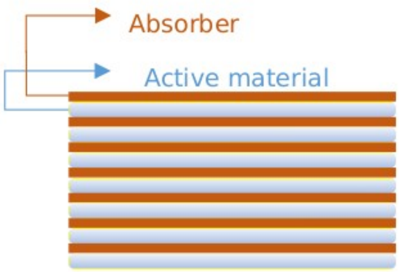


Why the FPGA is needed in R&D on DRC

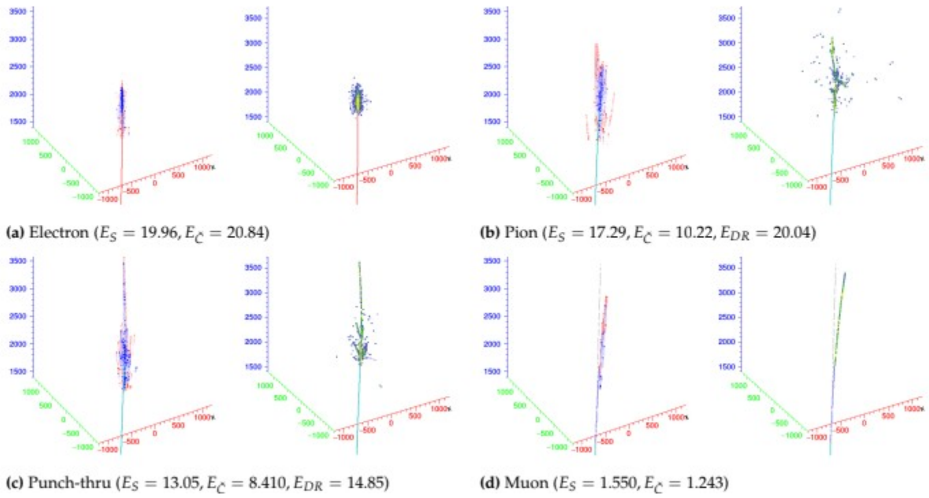
- Dual-Readout Calorimeter is longitudinal unsegmented calorimeter.
  - W/ time of Arrival information, longitudinal depth is reconstructed.
  - High granularity and good time resolution is required for 3D reconstruction of particle.
- Dual-Readout Calorimeter identifies the particle using time information.
- We decided to build the DAQ system using the DRS4 with a high sampling rate, and designed a customized FPGA-based DAQ to handle multiple channels.



General calorimeter



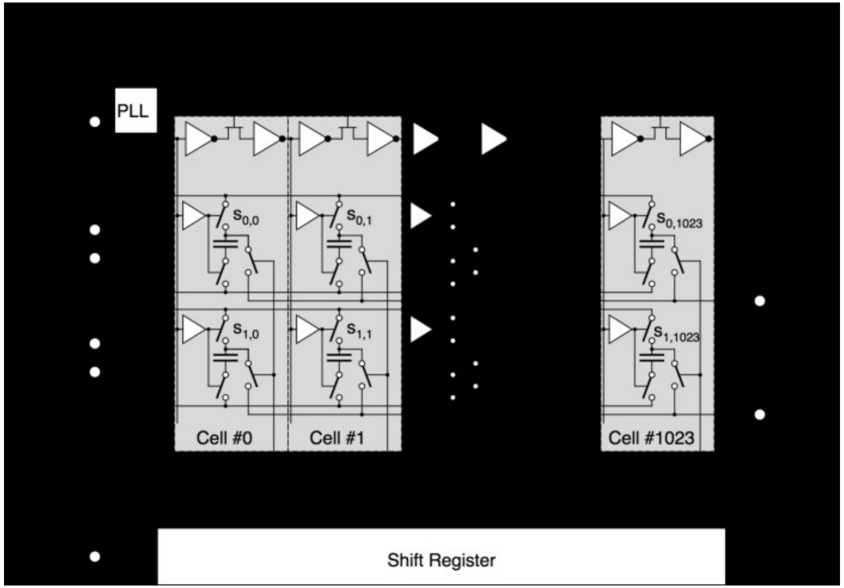
DRC

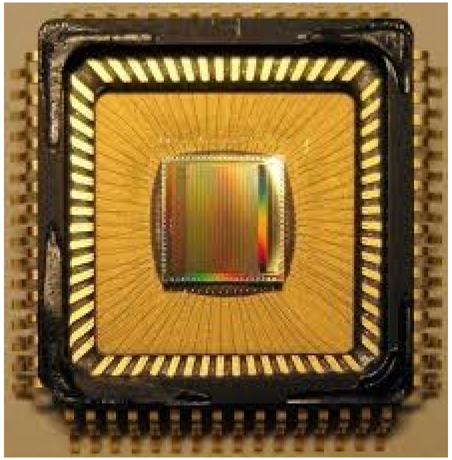


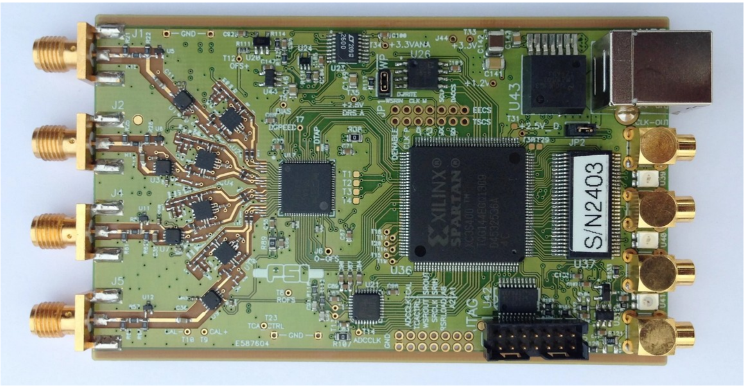
Simulaiton

Domino Ring Sampling (DRS4)

- Ultra-fast analog sampler up to 5 GSPS, using Switched Capacitor Array (SCA) technology.
- 9 input channels, each with 1024 sampling cells for waveform storage.
- Sub-10 ps timing resolution achievable after calibration (non-uniform bin size correction required).
- Compact and low-power (~50 mW/channel), efficient alternative to Flash ADCs.
- Widely used in HEP detectors, PET scanners, and fast timing applications.







Evaluation kit

Specification of DAQ system

- Our DAQ system consists of DAQ and TCB boards (NOTICE).

DAQ board

- Data AcQuisition board
- Each board cover 32 channels
- DRS4 chip

TCB board

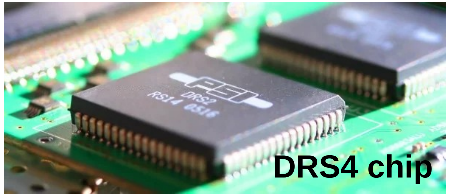
- Trigger and Clock Board
- Handles DAQ boards
- Set the all configuration

- DAQ specification

	Spec
Dynamic range	4096 ADC / 1 V
bins	1023

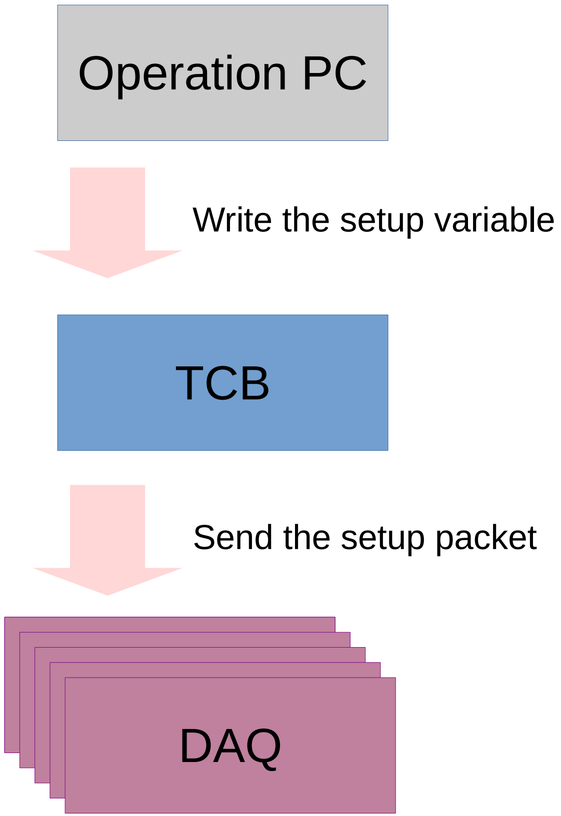
- Time window

Sampling	Time per bin	Total window (1023 bins)
5 GHz	200 ps	~ 200 ns
2.5 GHz	400 ps	~ 400 ns
1.25 GHz	800 ps	~ 800 ns



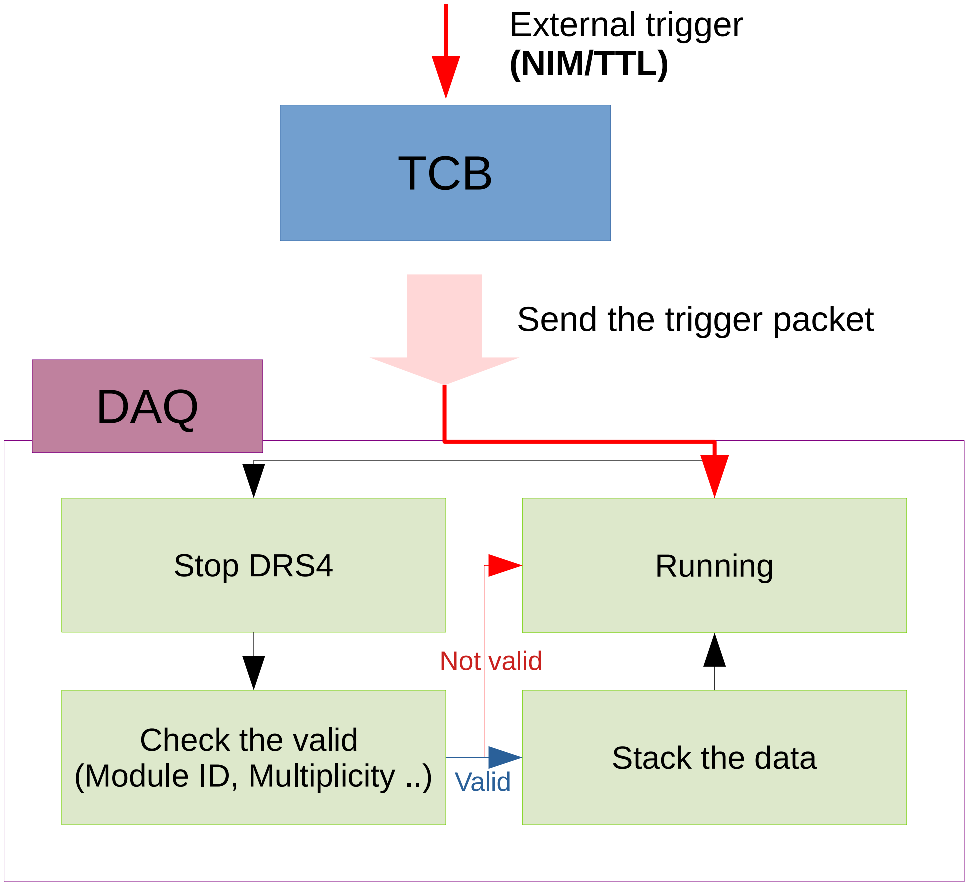
DRC DAQ system

Setting variable system



Check the setup packet w/ Module ID

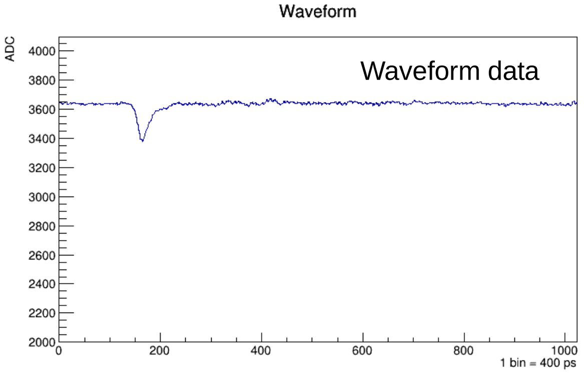
Trigger system

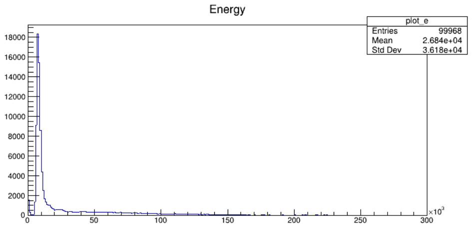


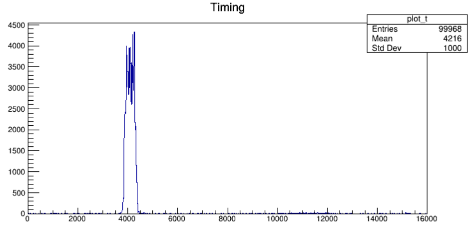
DAQ upgrade (Data acquisition mode)

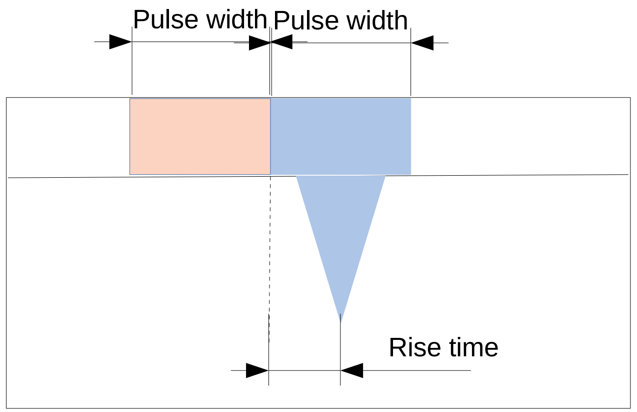
- Waveform mode
  - Save waveform data.
  - Data size is 960 kB in one event. **Heavy & slow but detail**
- Fast mode
  - Energy : integral waveform.
  - Timing : use leading edge method.
  - Data size is 3.75 kB in one event. **Light & fast**

4096 ADC = 1V

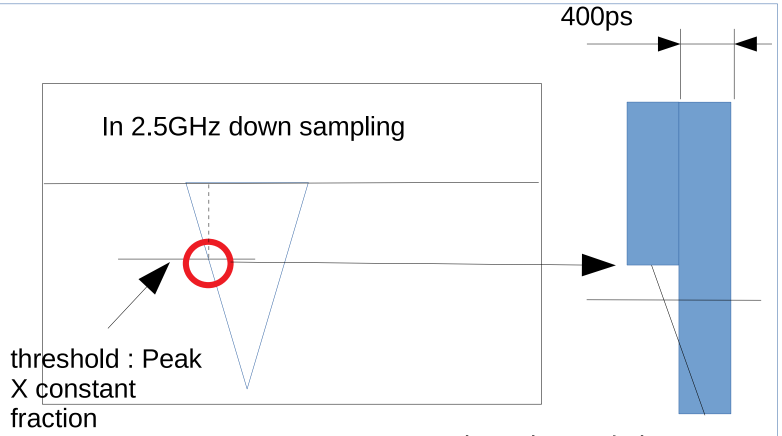








Energy = pulse + pedestal - pedestal

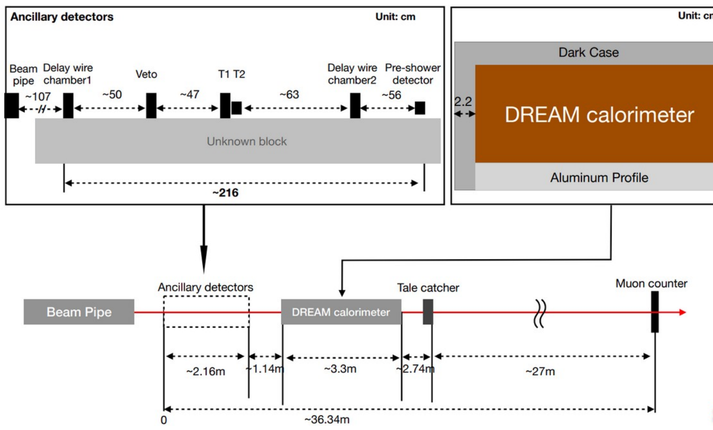


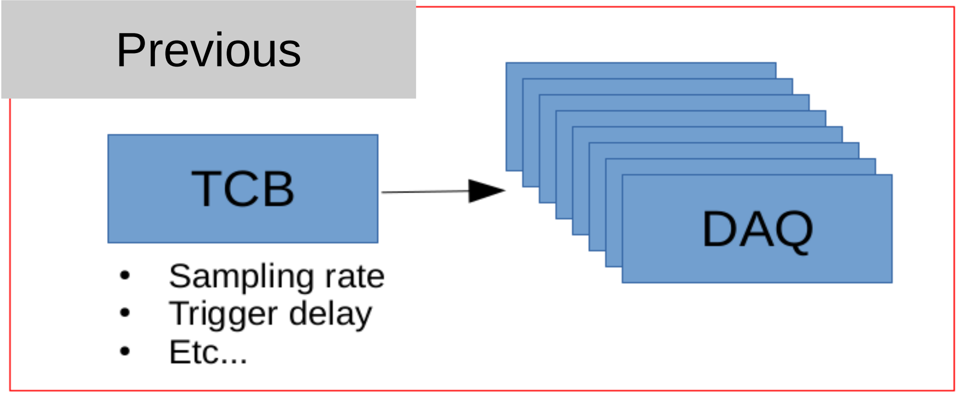
Linear interpolation
1 bin : 25 ps (bin size/16)

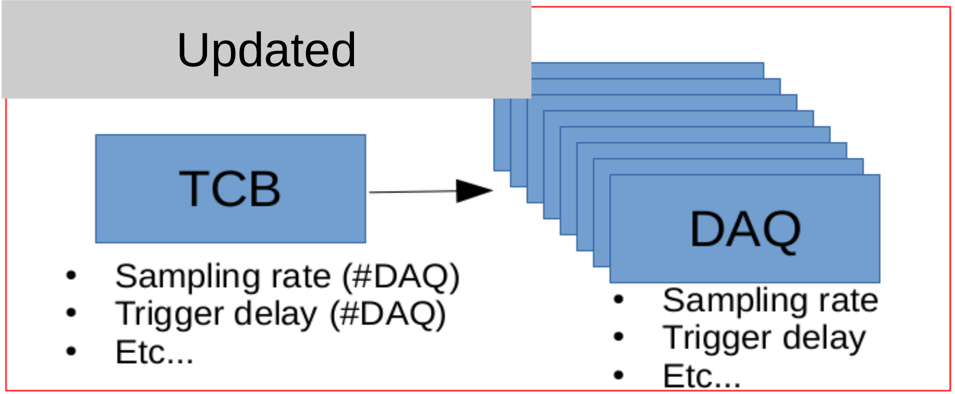
We prepared both mode!

DAQ upgrade (Time window)

- In test beam, in order to identify the particle and measure position, the various auxiliary detector.
  - Problem : because of cable latency and physical length, we cannot gather all signal in one window.
- Time window
  - Previous : Set the time windows in one variable (sampling rate & trigger delay) on TCB.
  - Updated : Set the time windows individually for each DAQ.







DAQ upgrade (time calibration)

- DRS4 : The chip process constraints lead to non-equidistant sampling bins in time.
- Time calibration
  - Measure and calibration the Δt of each sampling bins.
  - Add header the stopped bin of DRS.
  - Study is ongoing...

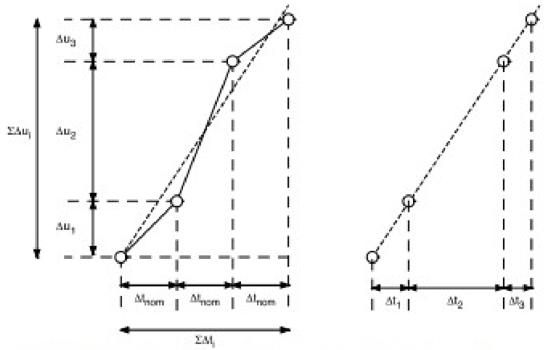


Fig. 3: The correlation between voltage differences Δu_i and time differences Δt_i of a rising edge can be used for the local TC of an SCA chip.

Local calib

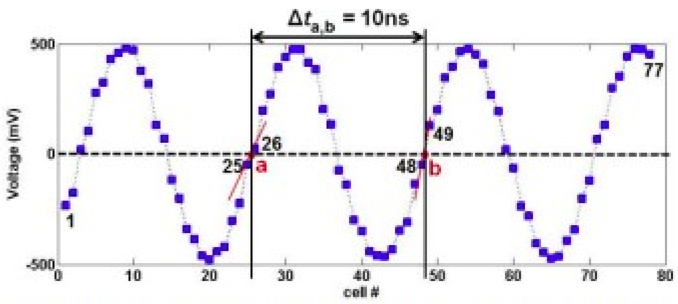
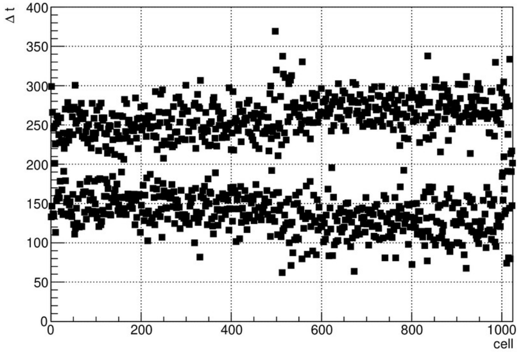


Fig. 4: First 77 cells of the 1024 cell array of a DRS4 sampling a 100 MHz sine wave at a sampling speed of 2.5 GSPS. This signal is used for the local TC and the global TC.

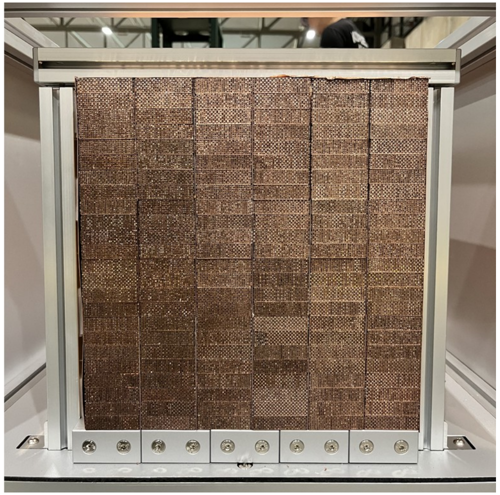
Global calib

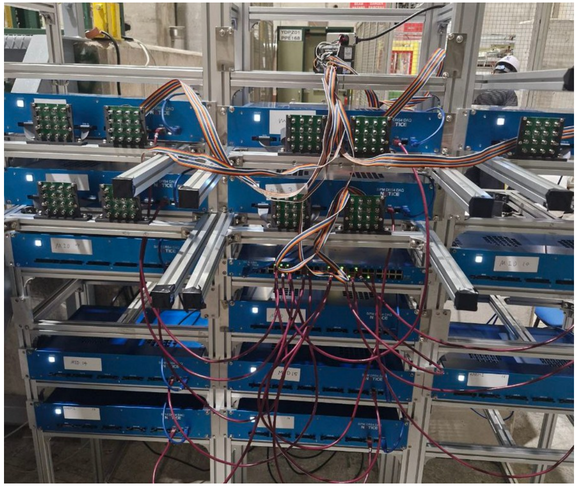


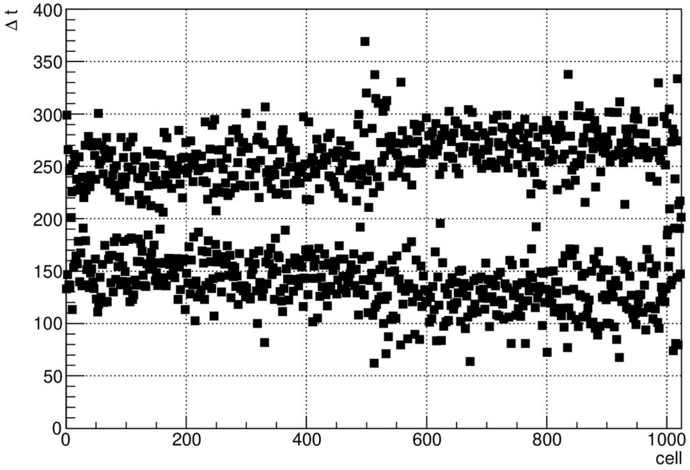
Δt distribution by bins

Summary

- We conduct the Dual-Readout Calorimeter R&D.
- The FPGA enables the implementation of a customized DRS4-based prototype DAQ system.
- We upgrade the prototype DAQ.
  - Design fastmode in order to prepare for high data rate.
  - Separate the time window individually by each DAQ boards.
  - Add stopped bin information for time calibration.







Back up

Remaining Firmware upgrade plan

- Apply the time calibration
- Upgrade the fastmode based on time calibration
- Etc...