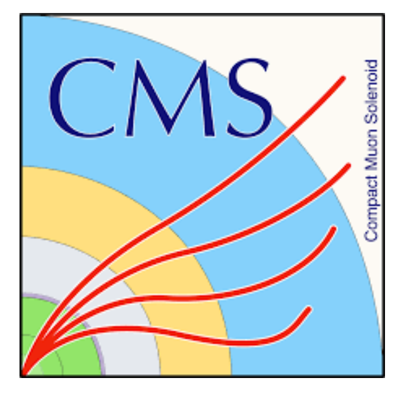
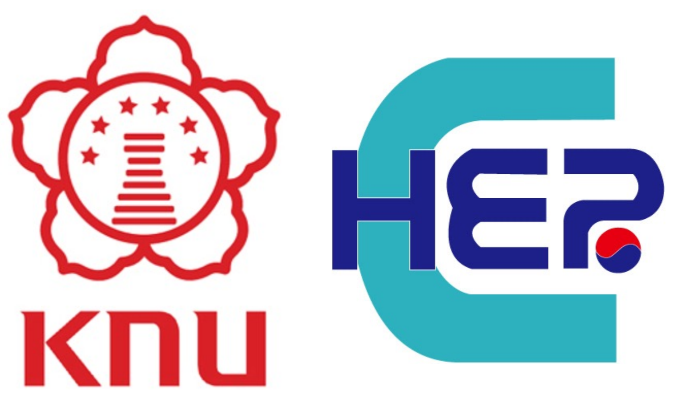



# Precision Timing at High-Luminosity LHC with the CMS MIP Timing Detector

*CHANG-SEONG MOON*

*CENTRE FOR HIGH ENERGY PHYSICS (CHEP),* KYUNGPOOK NATIONAL UNIVERSITY (KNU)

KSHEP 2024 Spring Meeting, May 24 2024

# High-Luminosity LHC at CERN

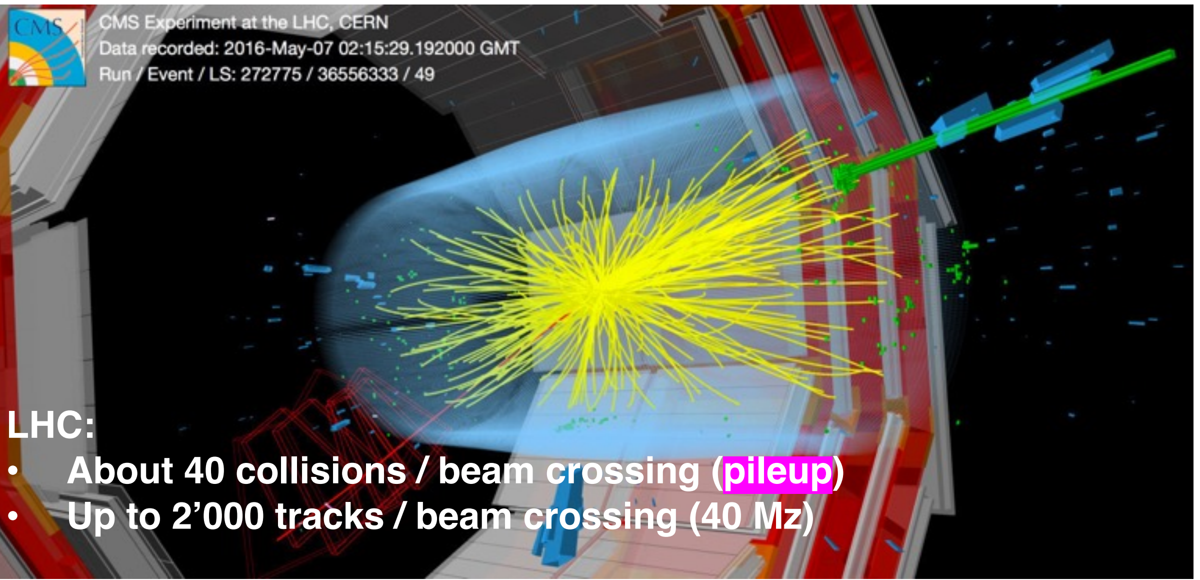
Goal: precision tests of the standard model and Higgs physics, and searches for (rare) BSM phenomena

- **Precision measurement of Higgs boson couplings** (few percent)
- Measurement of the **Higgs boson self-coupling** via direct observation of the di-Higgs boson production
- Search for heavy **dark matter candidates, SUSY particles, new gauge bosons, Long-Lived Particles**, …

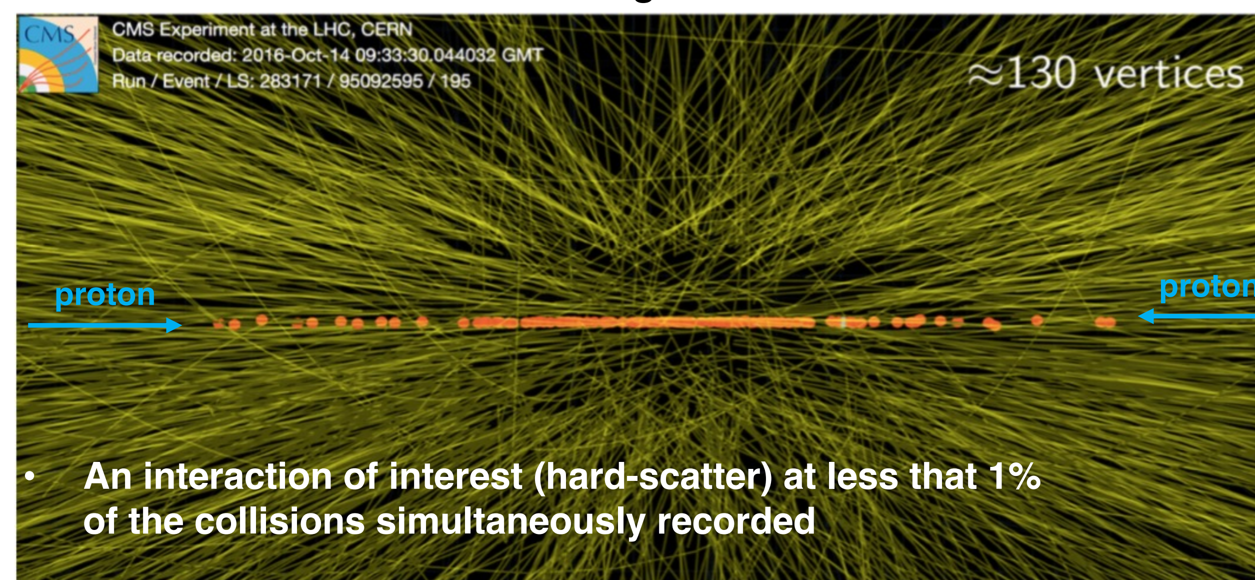
Means: upgrade of the LHC optics and injectors to increase the beam intensity

- Luminosity delivered by **LHC** (2009-2025): **~ 400 $fb^{-1}$ / experiment** *[~250 $fb^{-1}$ collected so far]*
- Target luminosity for **HL-LHC** (2029-2042): **>3000 $fb^{-1}$ / experiment** ***[one year of HL-LHC equivalent to ~10 years of LHC]***

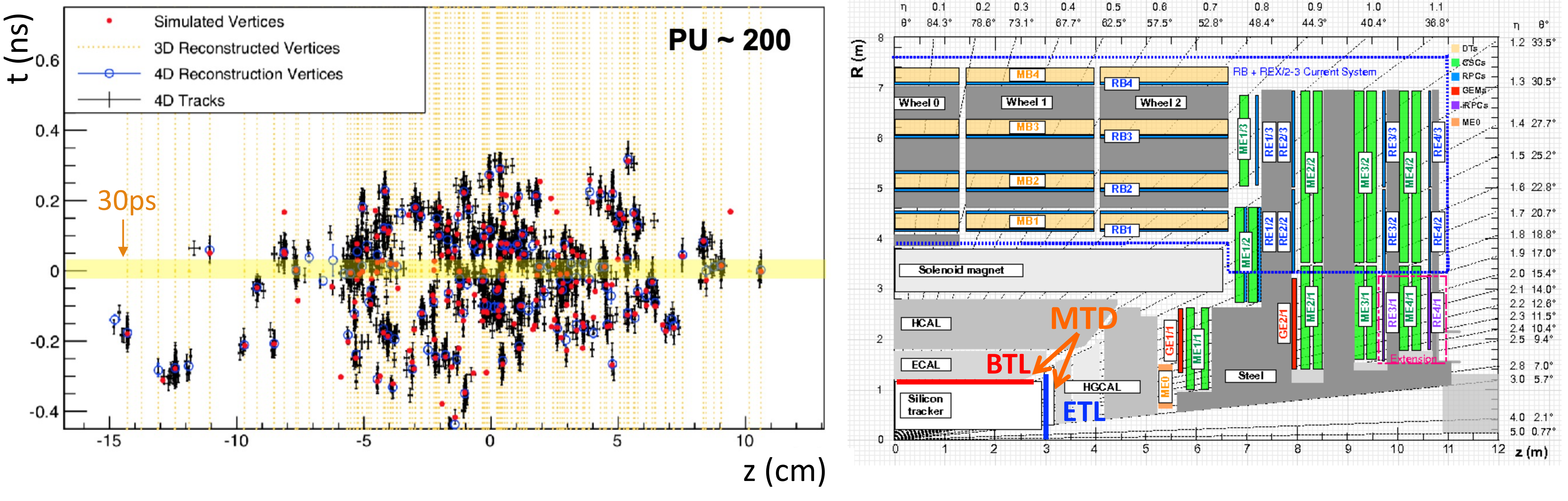
**Collision event with 35 reconstructed vertices**




**Real life event at the LHC emulating HL-LHC conditions**

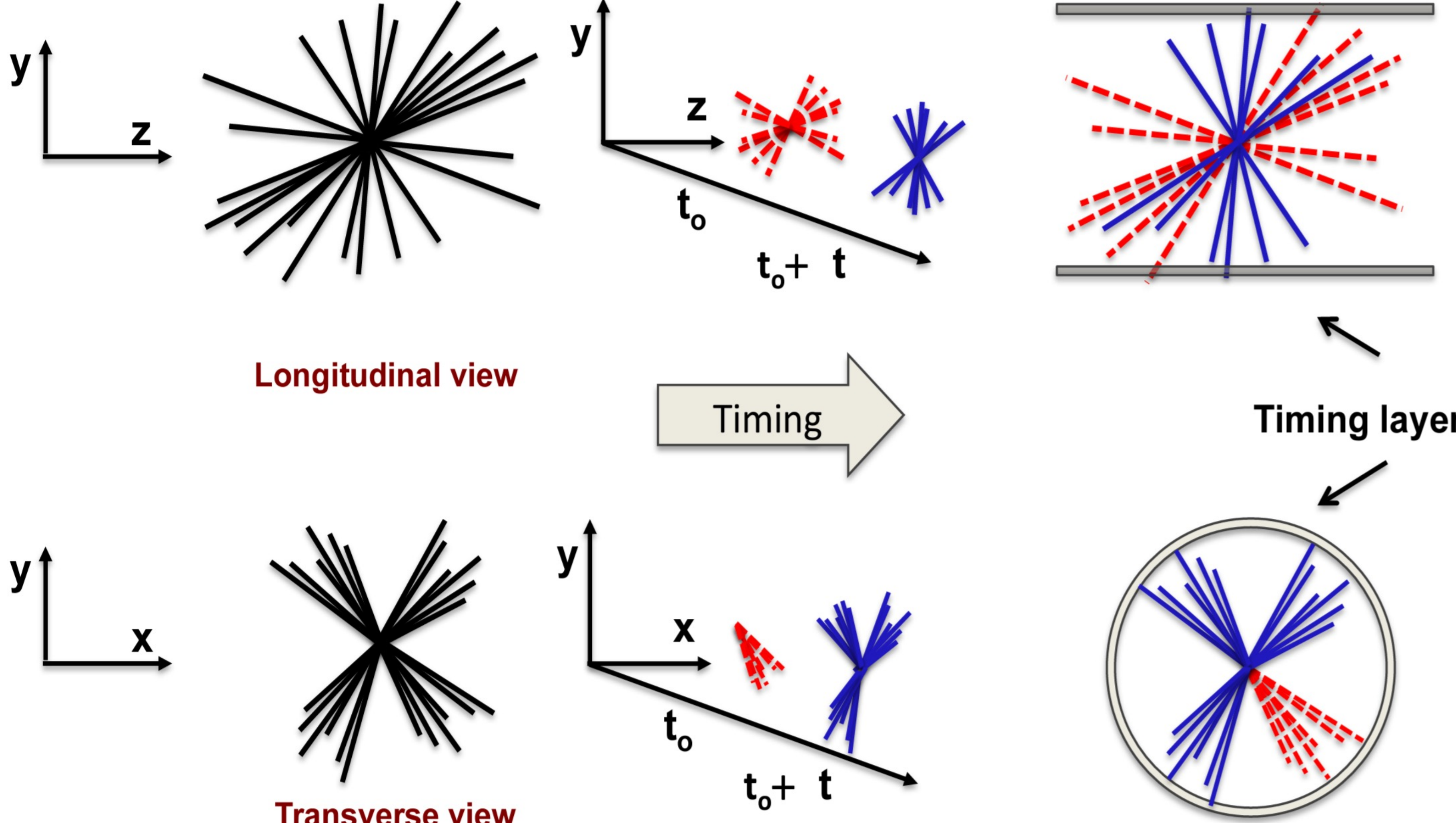


# MIP Timing Detector (MTD) for CMS Phase-2 Upgrade




- Important to maintain detector performance during HL-LHC running
  - Time information will help to reduce pileup effects from approximately 200 simultaneous interactions
- MIP timing detector (MTD) consists of barrel timing layer (BTL) and endcap timing layer (ETL), providing 30-50 ps time resolution per track
  - BTL: LYSO crystal scintillator + SiPM readout
  - ETL: Silicon based sensor (LGAD) + ASIC readout
  - Two different detector technologies for radiation hardness and costs

# New concept: Tracking in 4 Dimension

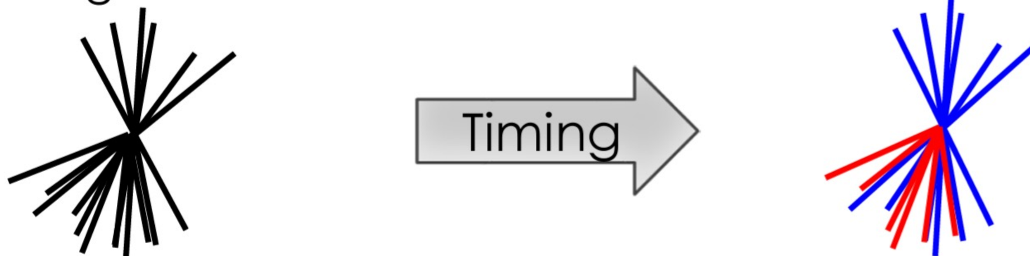



N. Cartiglia

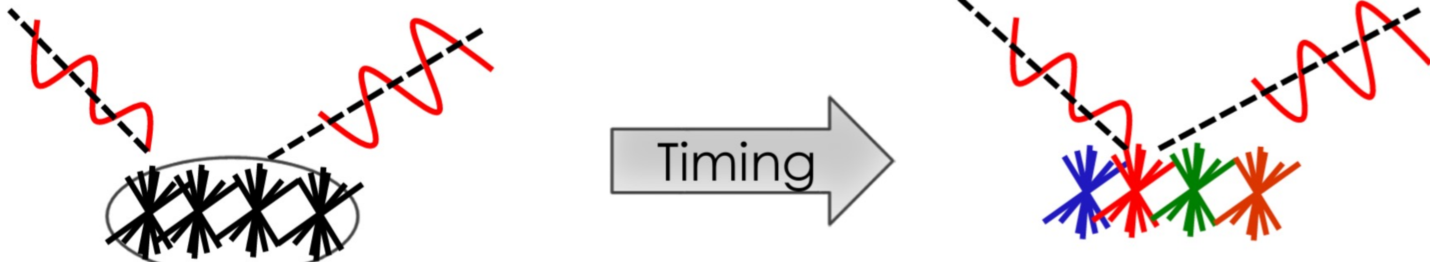
- Timing allows separating collisions that happen in the same location

# Timing in the event reconstruction

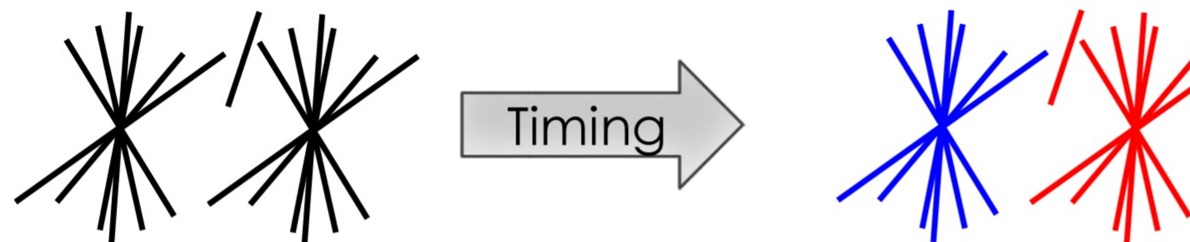
**Missing Et:** consider overlapping vertexes, one with missing Et: Timing allows obtaining at HL-LHC the same resolution on missing Et that we have now




**H ➔ γ γ :** The timing of the γγ allows to select an area 1 cm) where the vertex is located. The vertex timing allows to select the correct vertex within this area



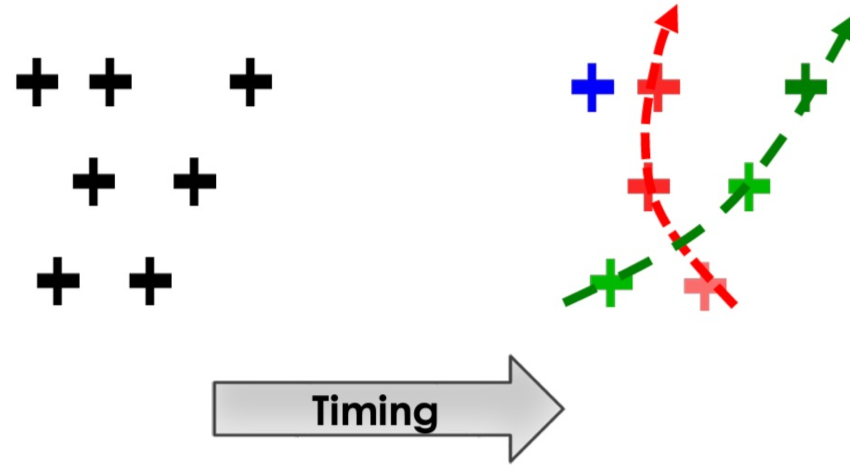

**Displaced vertexes:** The timing of the displaced track and that of each vertex allow identifying the correct vertex

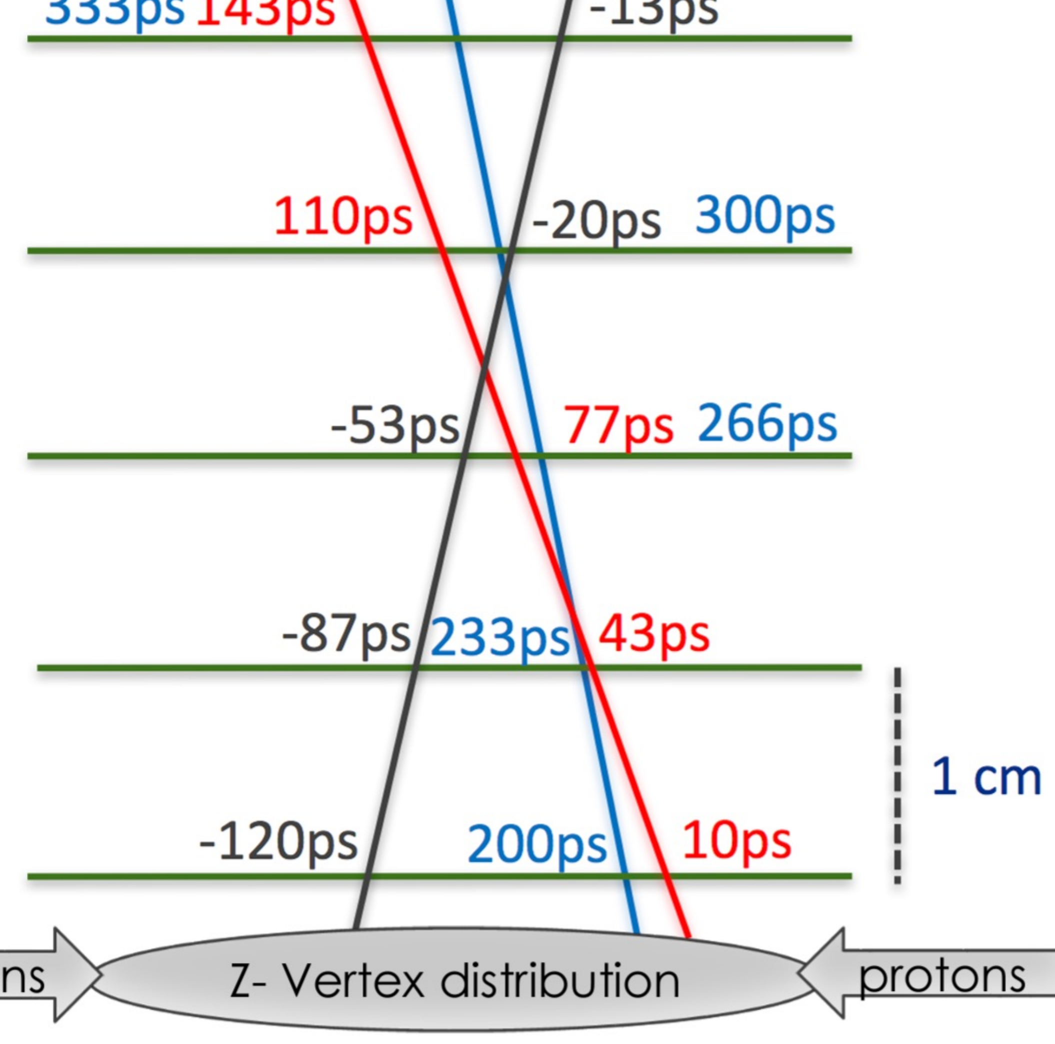



N. Cartiglia

# 4D tracking: Timing at each hit point

- Massive simplification of patter recognition, new tracking algorithms will be faster even in very dense environments
- Use only "time compatible points"

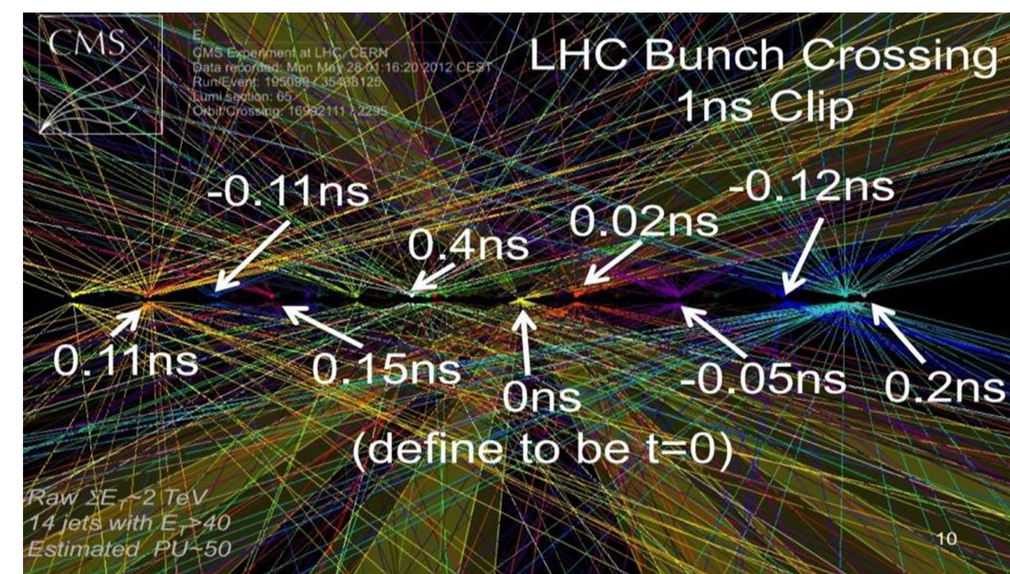



"**4D tracking**"
: the process of assigning a space and a time coordinate to a hit.

N. Cartiglia

# MTD Physics motivation: pile-up mitigation




Spurious pile-up jet

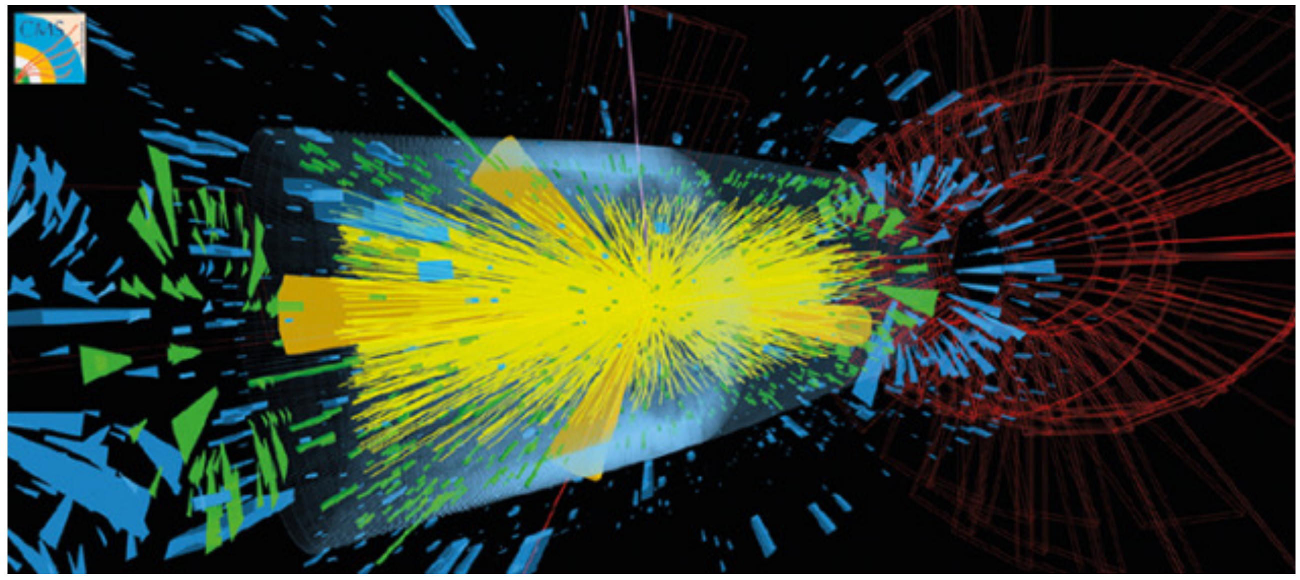
Hard-scatter jet

Jet from pile-up

Pile-up

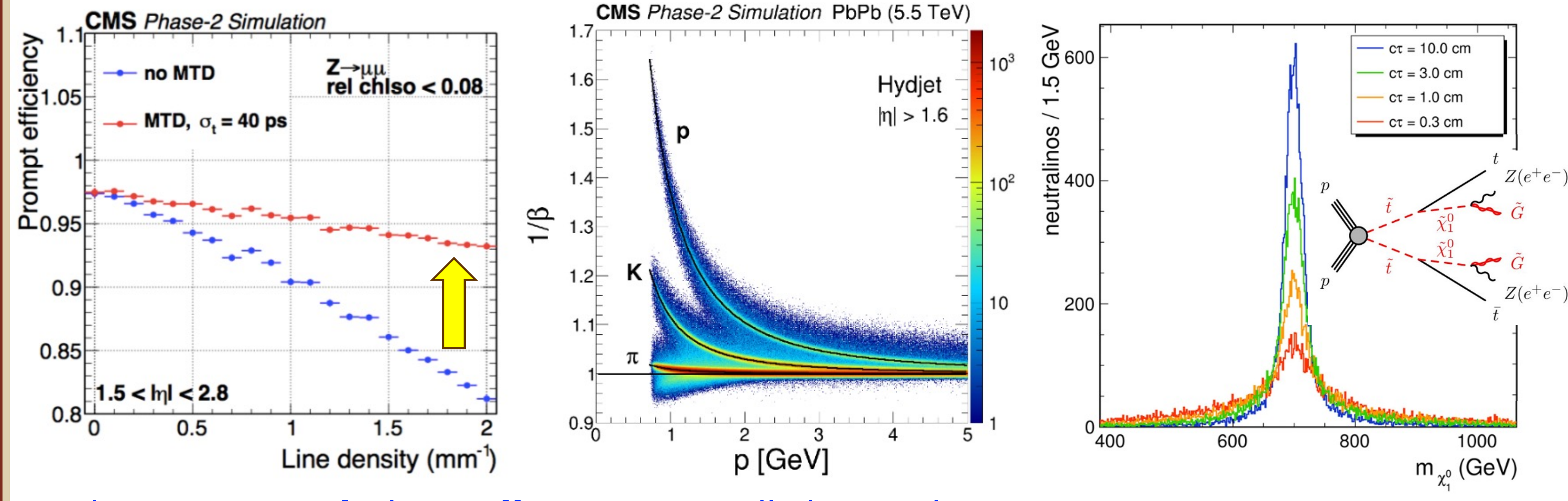
Hard scatter

- Important to maintain detector performance during HL-LHC running
  - Time information will help to reduce pileup effects from approximately 200 simultaneous interactions




The display of an event with a Higgs boson produced in the VBF process on top of 200 pile-up collisions.

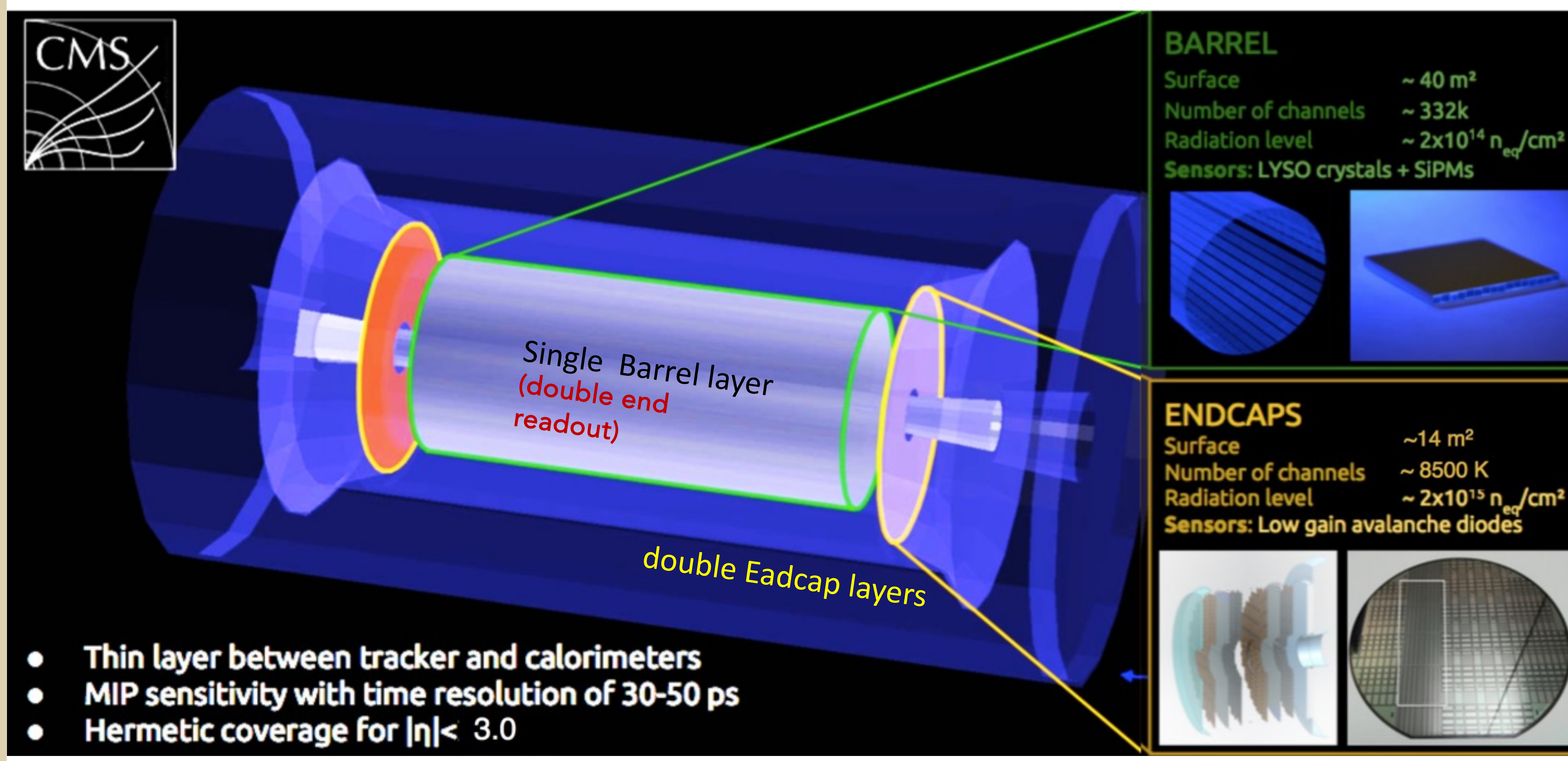
# MTD Physics impact on CMS Physics Program




- The mitigation of pile up effect improves all physics objects
- 4D vertexing (position + time) can remove
  - Spurious pileup tracks from "isolation cone" around leptons
  - Spurious jets formed from pileup particles.
- MTD can provide significant improvement for particle ID: Heavy ion charm tag
- Significant gains for searches for long-lived new particles

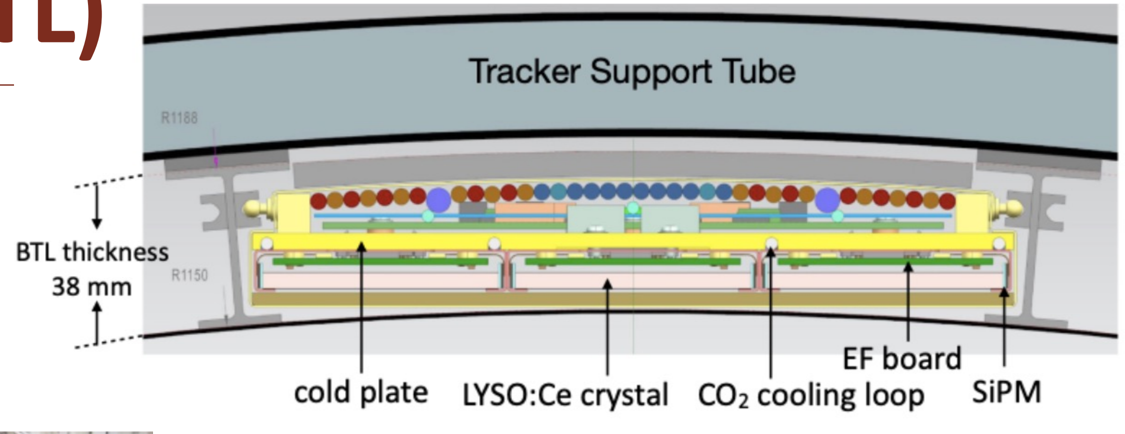

CHANG-SEONG MOON (KNU)

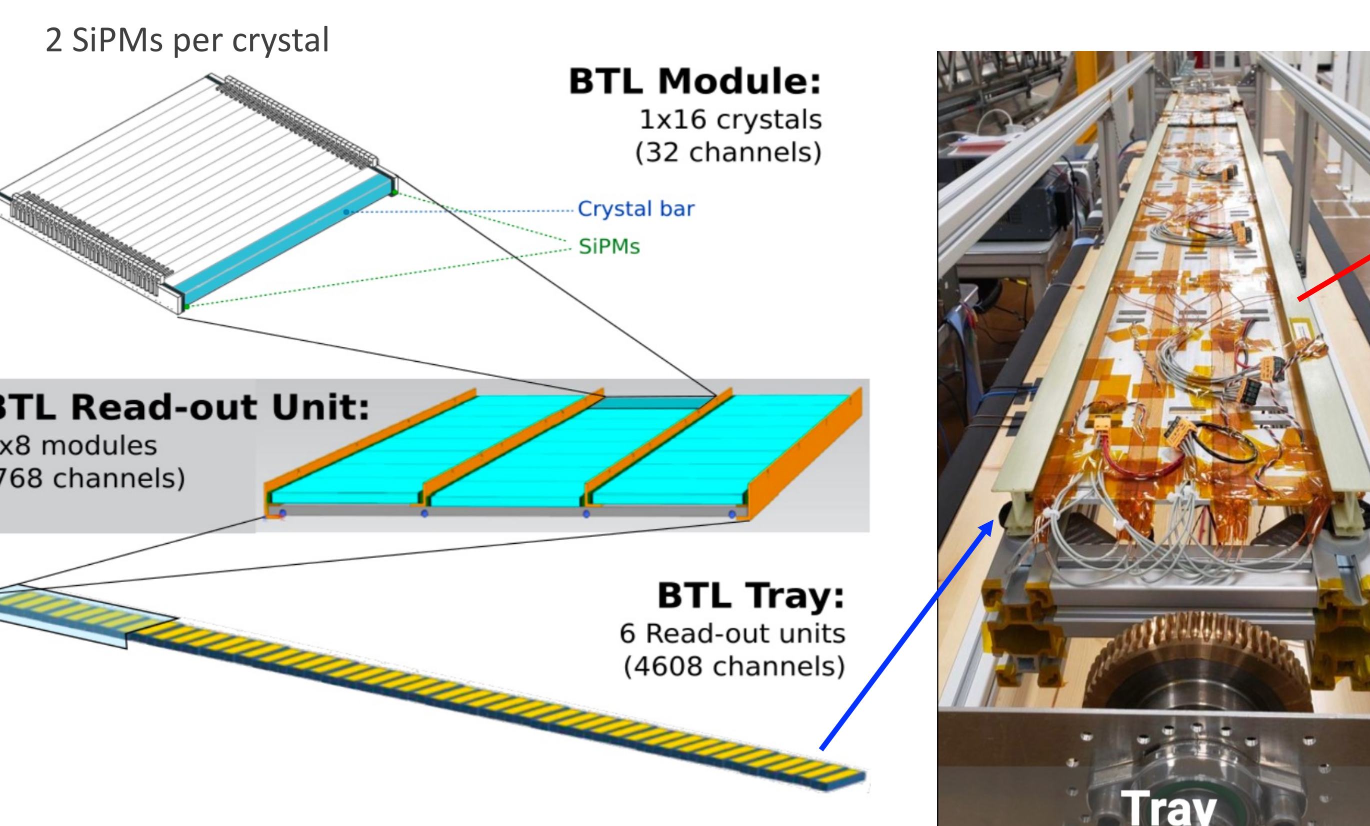
# Mip Timing Detector (MTD)



# MTD Barrel Timing Layer (BTL)

- 3.8 cm thin cylindrical detector
  - located inside the tracker support tube, |η| < 1.45
  - ~5 m long, 38 $m^2$ surface

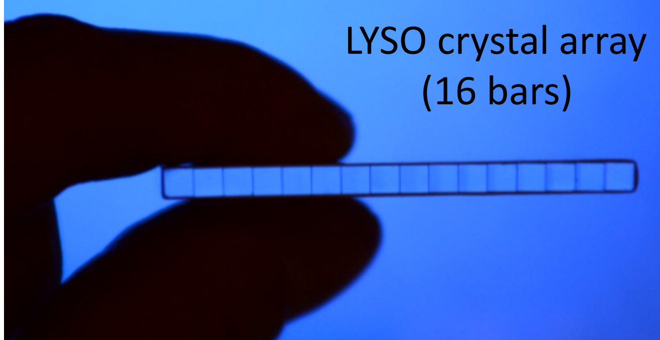


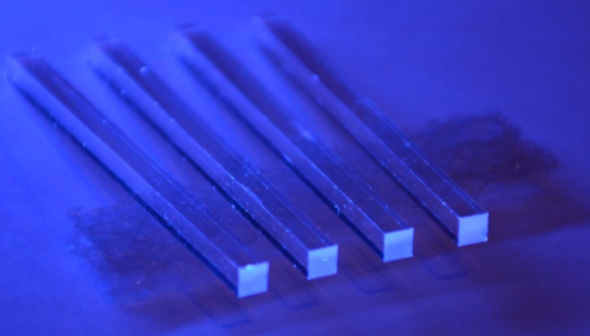



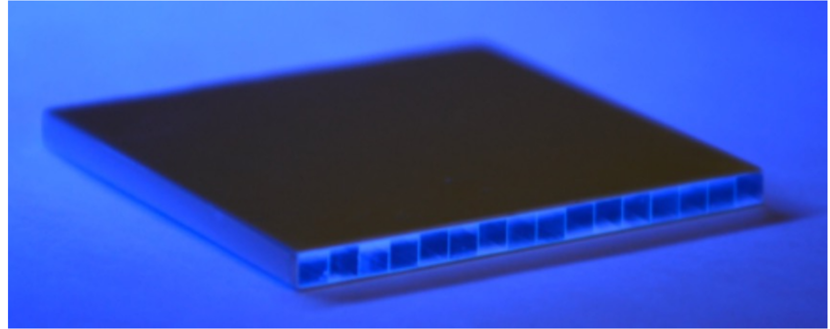
- BTL construction: starting in early 2024!

# BTL sensors : LYSO crystal

- LYSO crystal bars (166k)
  - Cerium-doped lutetium yttrium orthosilicate (LYSO:Ce) scintillation medium
  - Well established in PET applications and vendors widely available
  - High radiation tolerance
  - $\tau_{rise}$ : ~100 ps, $\tau_{decay}$ : ~ 40 ns
  - High Light Yield : 40000 γ/MeV

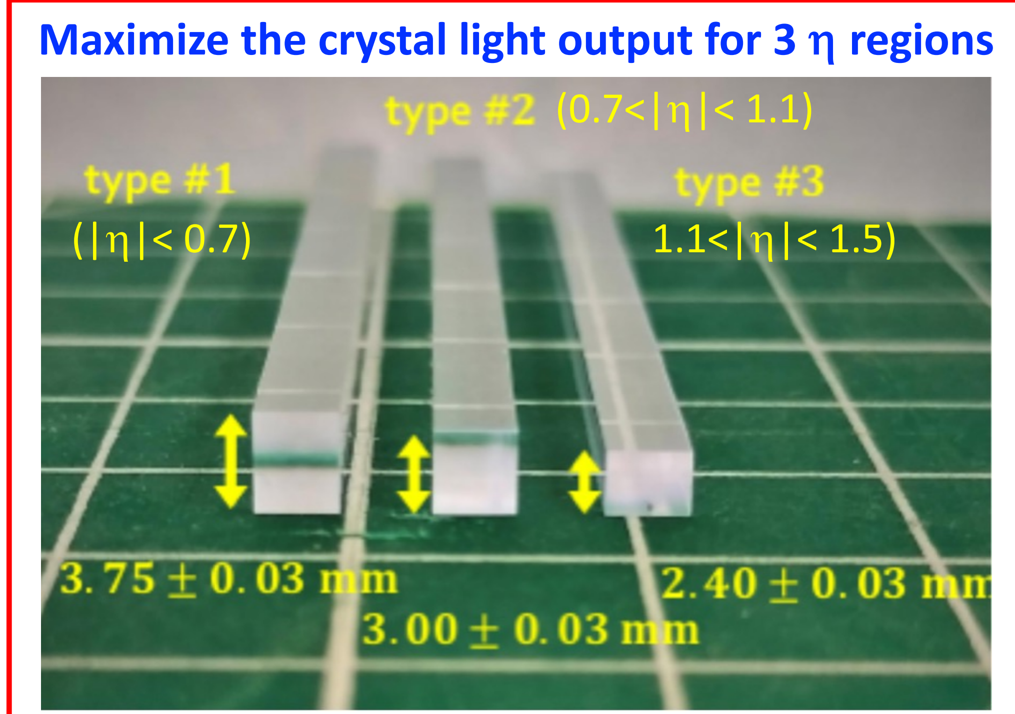




- LYSO current status
  - Single vendor selected
    - Considerably better offer
    - One of best vendor for performance-wise
    - Reliable vendor (large production capacity)
  - Pre-production in progress
    - Ordered in March (2% of the total LYSO arrays)
    - QA/QC and construction database ready

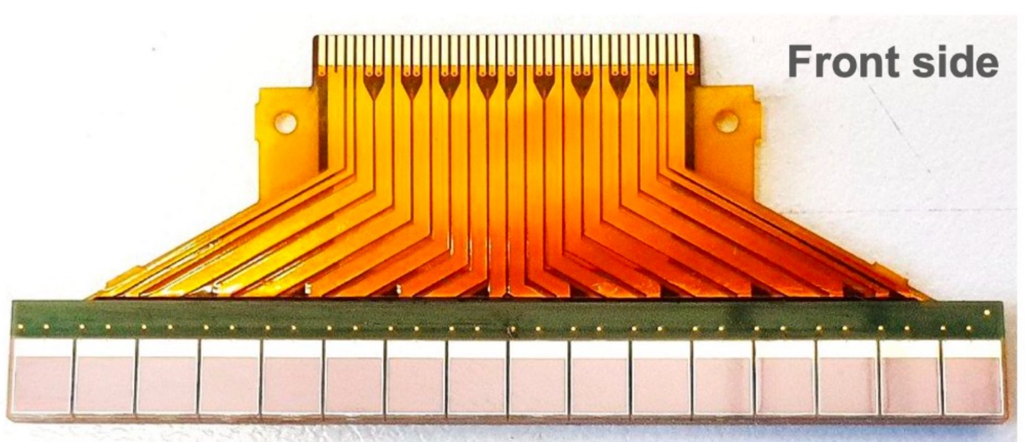
**Maximize the crystal light output for 3 η regions**

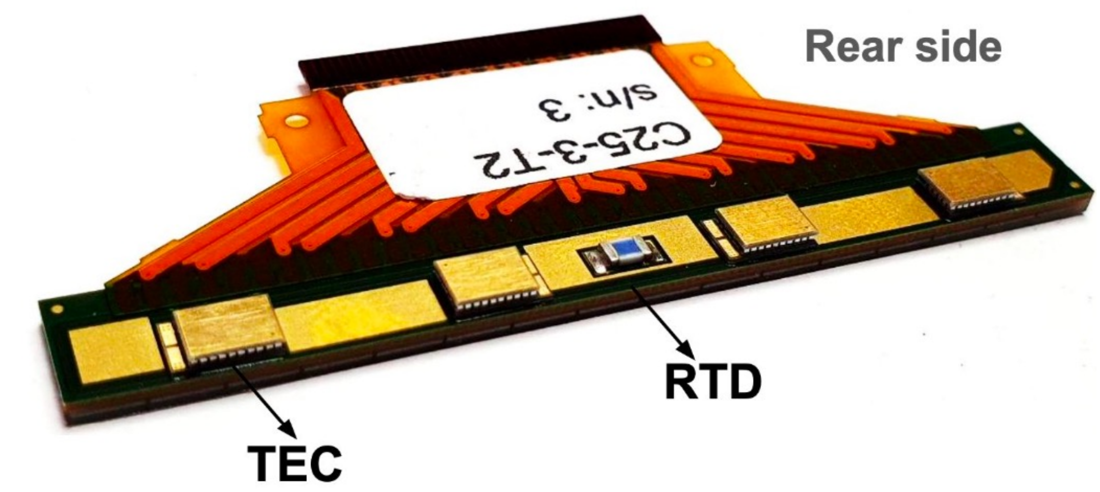


# BTL sensors : SiPM

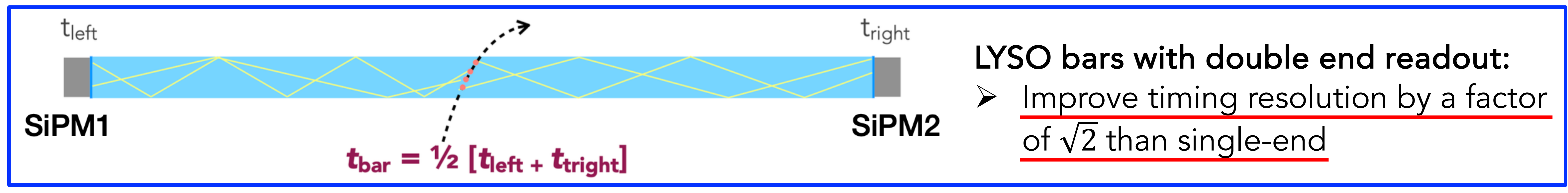
- SiPM (166k x 2 = 332k channel)
  - Well consolidated technology
  - Photon Detection Efficiency (PDE) : 20–40%
  - Compact, robust, insensitive to magnetic fields
  - Good radiation hardness
  - Fast recovery time <10 ns
  - High dynamic range ($10^5$)
- SiPM current status
  - Optimized cell size (25 μm) as a default for BTL
    - Additional performance gain to boost signal
  - SiPM die size ($3.8 \times 2.9$ mm$^2$) fixed to match with the thickest LYSO geometry
- SiPM plans
  - Tender starts in July
  - Sign the production contract in September
  - First batch delivered ~ Feb. 2024 (for 7 months)

SiPM Module



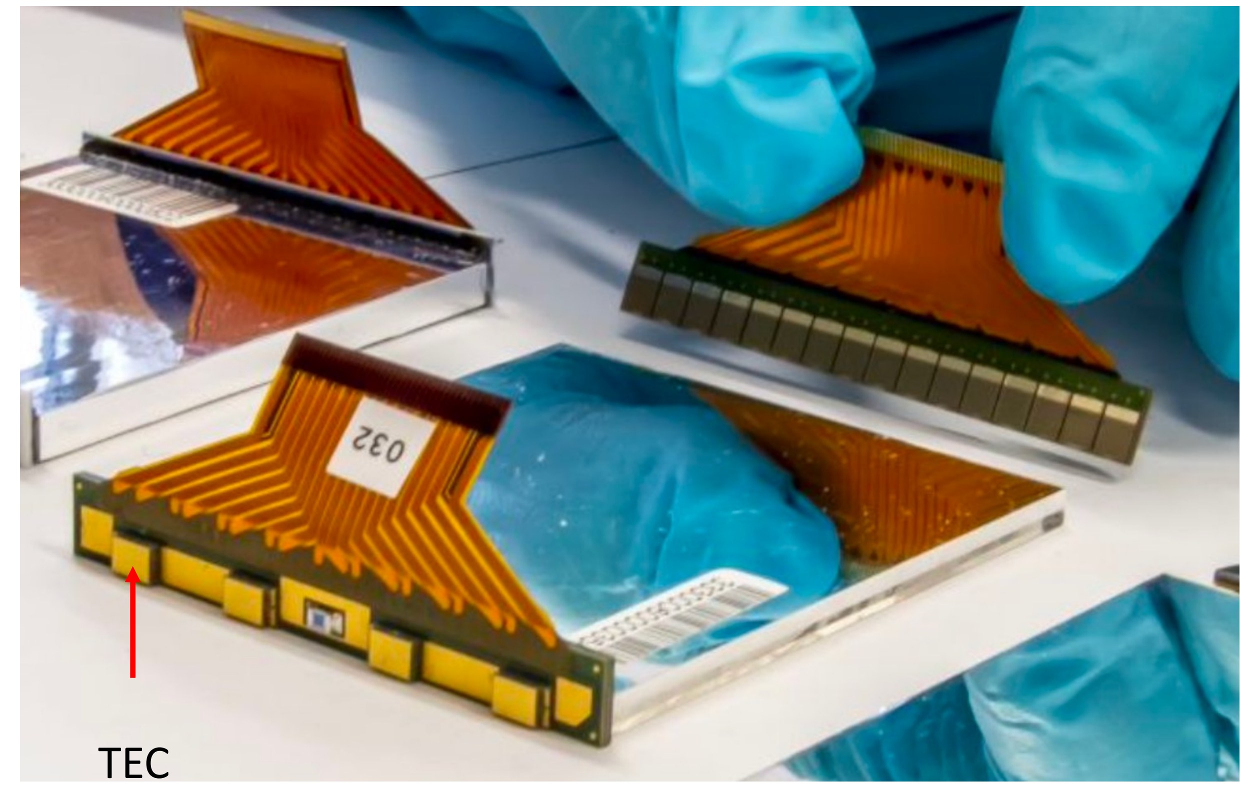
# BTL sensors : LYSO crystal and SiPM

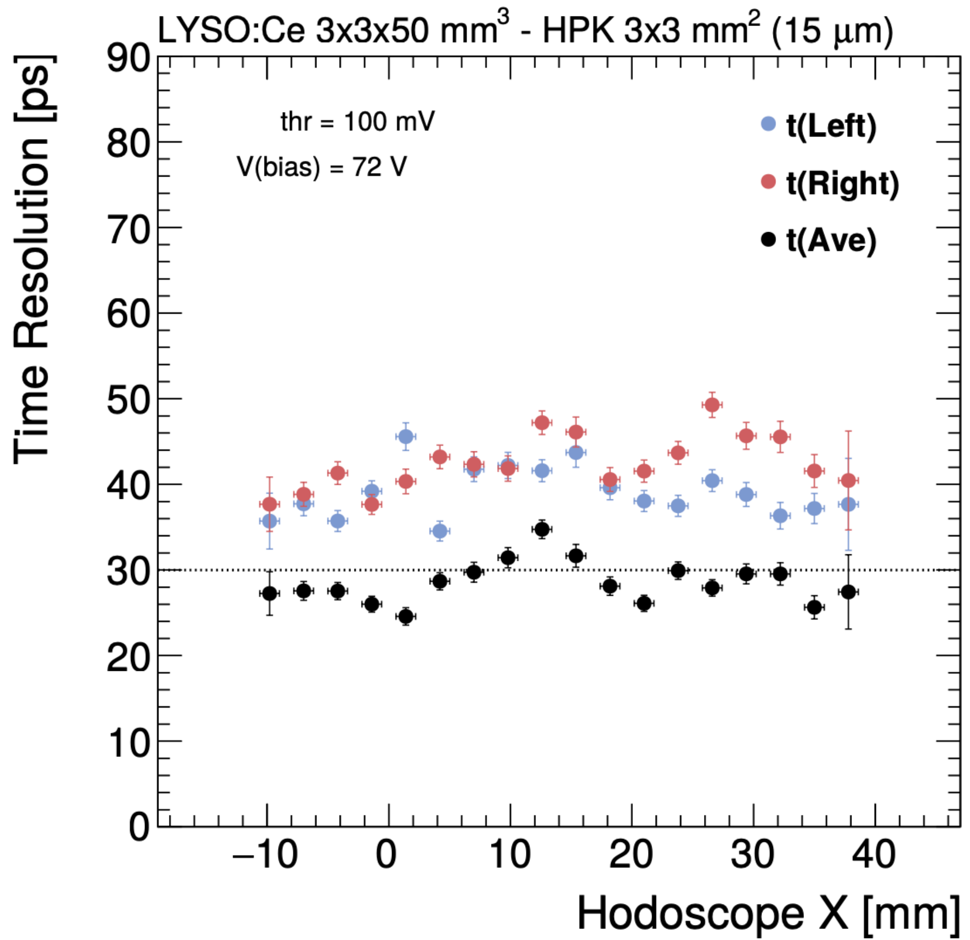



**LYSO bars with double end readout:**

- Improve timing resolution by a factor of $\sqrt{2}$ than single-end

## Sensor Module (LYSO + SiPM & TEC)



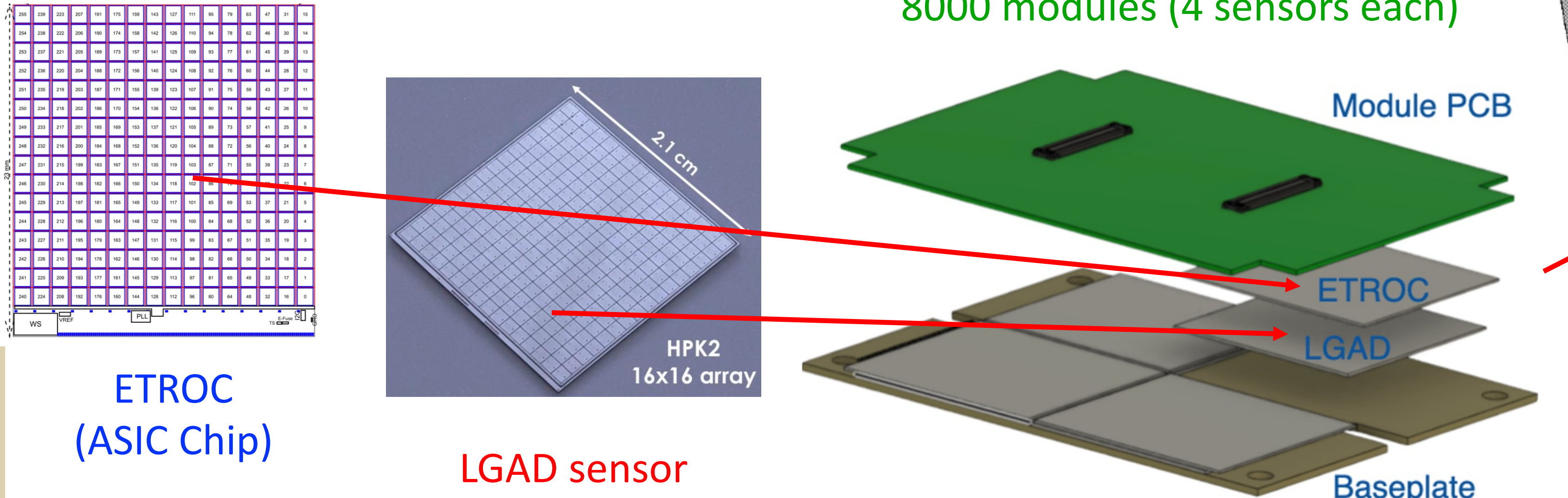



# MTD Endcap Timing Layer (ETL)

- Two double- sided disks for each side
  - Maximize geometrical acceptance (85% per disk)
  - Coverage : 1.6 < |η| < 3.0
  - Average of 1.8 hits per track
  - **Time resolution per track < 35 ps**
    - based on single hit resolution < 50 ps
- Low-Gain Avalanche Diode (LGAD) sensor bump bonded readout ASIC (ETROC)

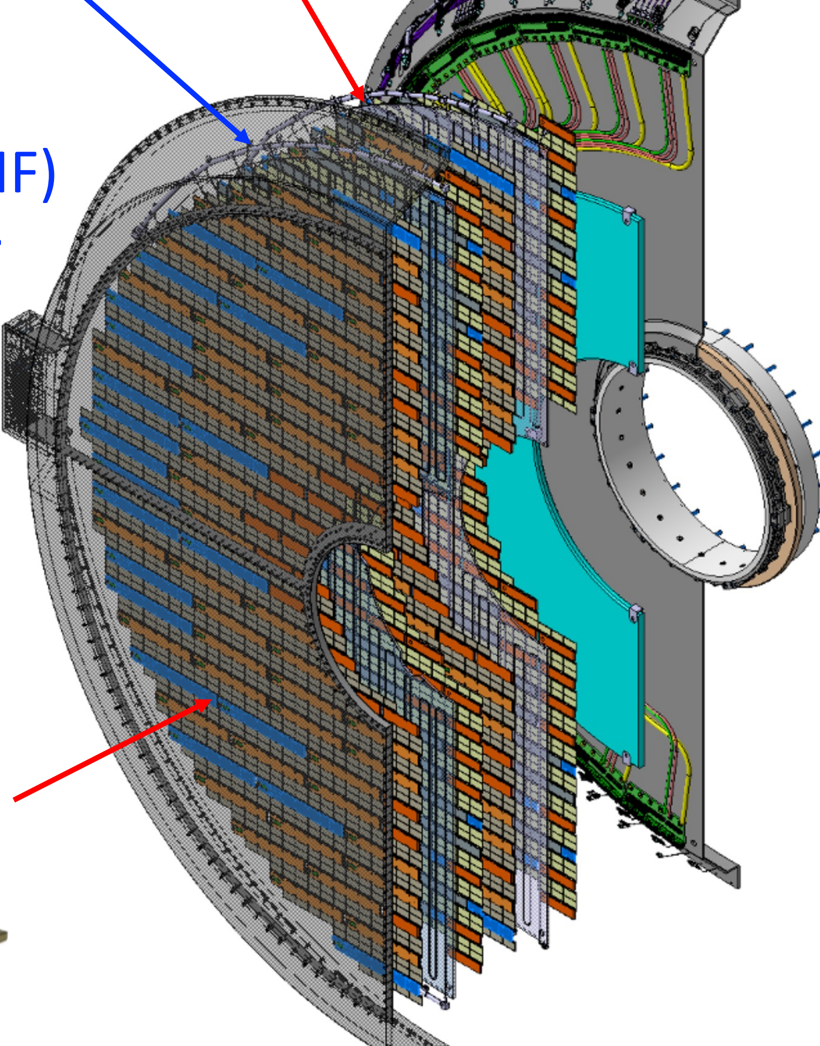
7330 sensors
for each disk (905 kCHF)
-> 123 CHF per sensor

8000 modules (4 sensors each)




ETROC
(ASIC Chip)

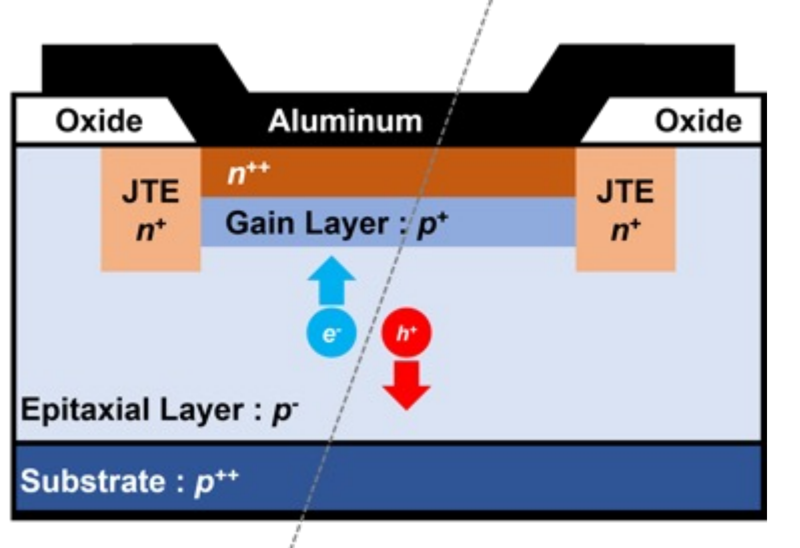
LGAD sensor

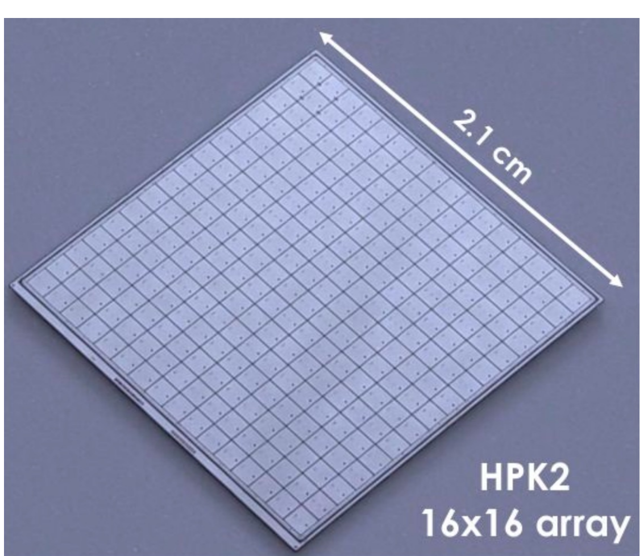



31.5 cm < radius < 120 cm

# Low Gain Avalanche Diode (LGAD) sensors

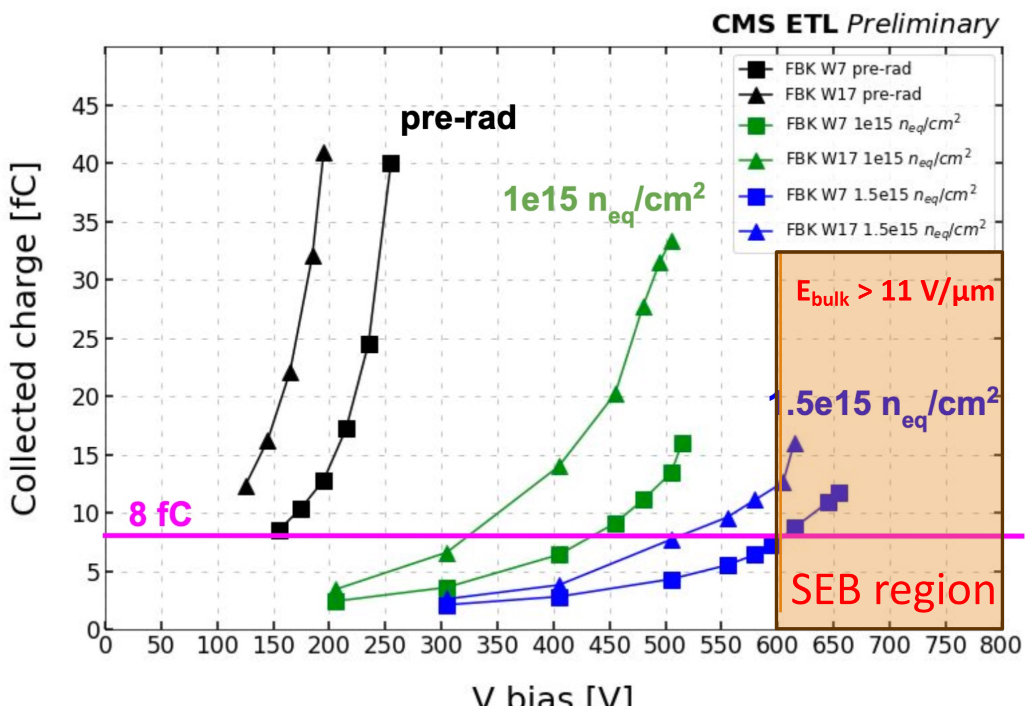
- LGAD characteristics (16x16 pixel matrix, 1.3x1.3 $mm^2$ pixel size)
  - Precision position reconstruction and timing resolution
  - Highly improved radiation tolerance
  - Moderate gain factor (10-30) to maximize S/N ratio -> Large signals with low noise
  - Thin implanted gain layer of overall thickness of 35–50 μm
  - Gain uniformity (>8 fC of charge)
- The additional Gain layer: highly boron-doped thin layer at the n-p junction
  - Generates the high field necessary to achieve charge multiplication.

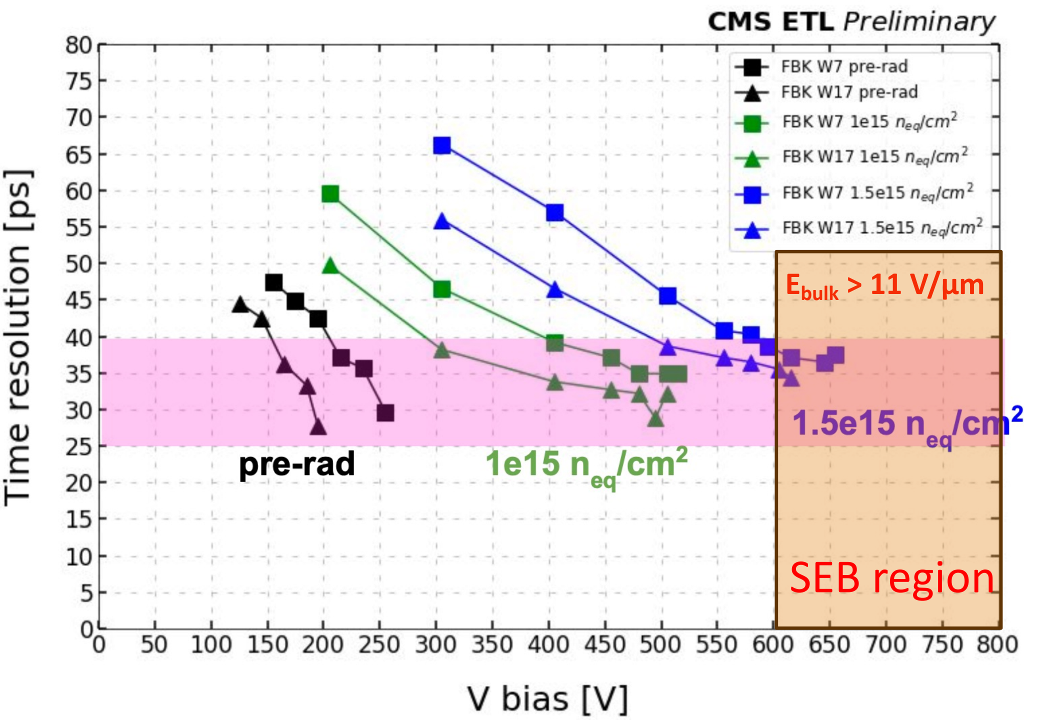


# Performance tests for LGAD sensors

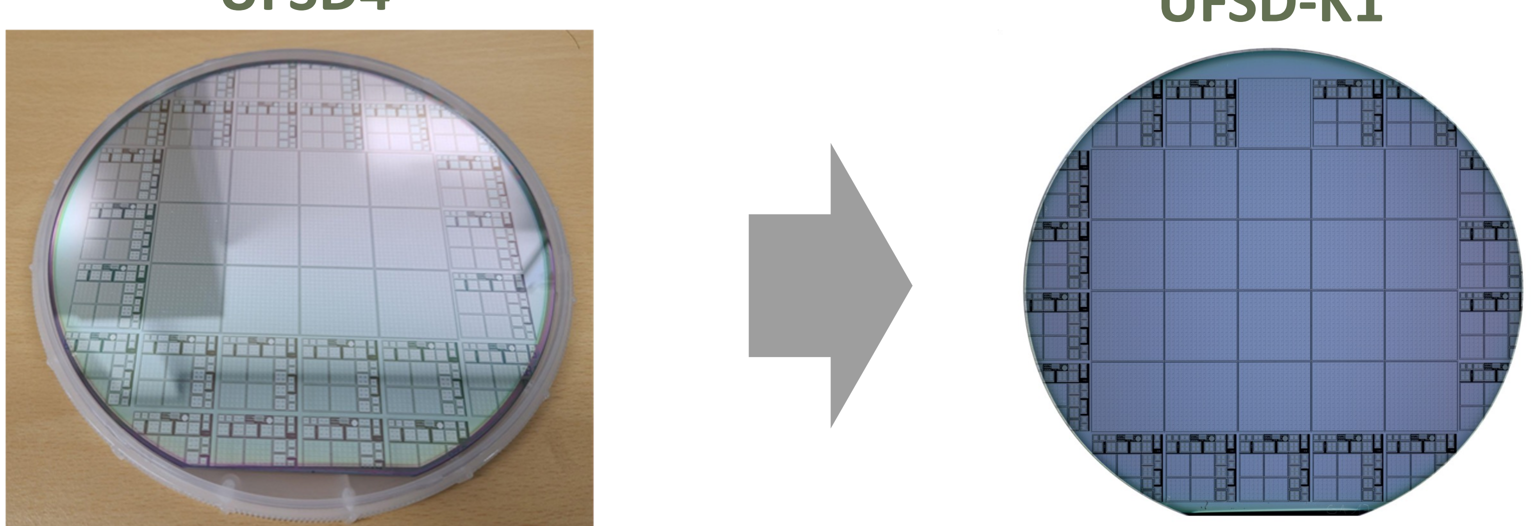
- Completed Market Survey for the procurement of the final LGADs Prototype.
  - Qualified 4 vendors for production of the final LGAD sensors
- Irradiated FBK sensors measured with a beta-source (Sr90) setup
  - Collected charge and time resolution was satisfied with requirements
  - Fully recover performance by increasing the bias voltage
- Single Event Burn-out (SEB) observed for $E_{bulk} > 11$ V/μm



# UFSD-K1 wafer from FBK in Italy

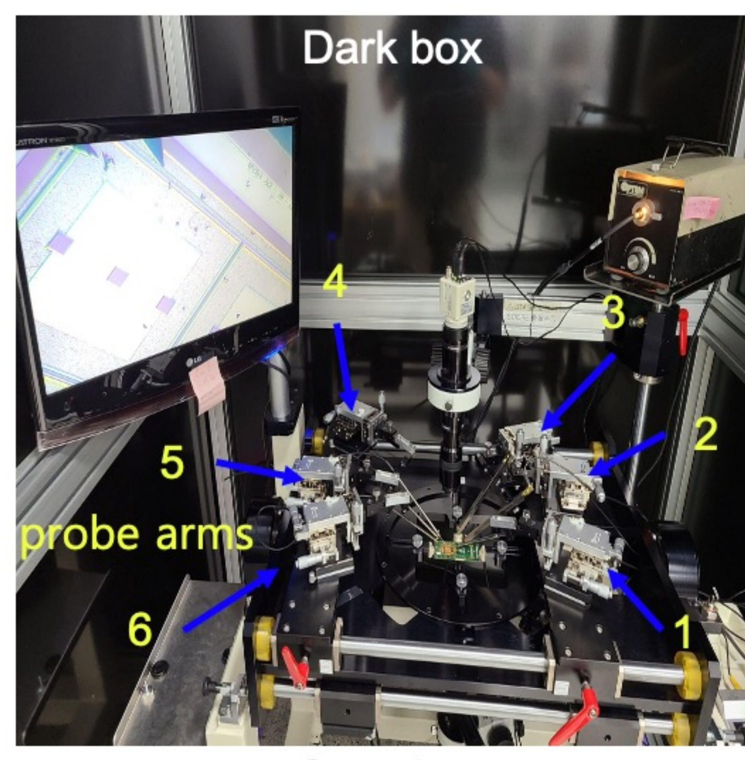
- The UFSD-K1 is the latest version of UFSD (Ultra-Fast Silicon Detectors) ordered from Korea.
- Fifteen number of UFSD-K1 wafers manufactured by two different wafer suppliers have been delivered to KNU.
- Wafer-level test of the UFSD-K1 is underway to compare performance between two suppliers.



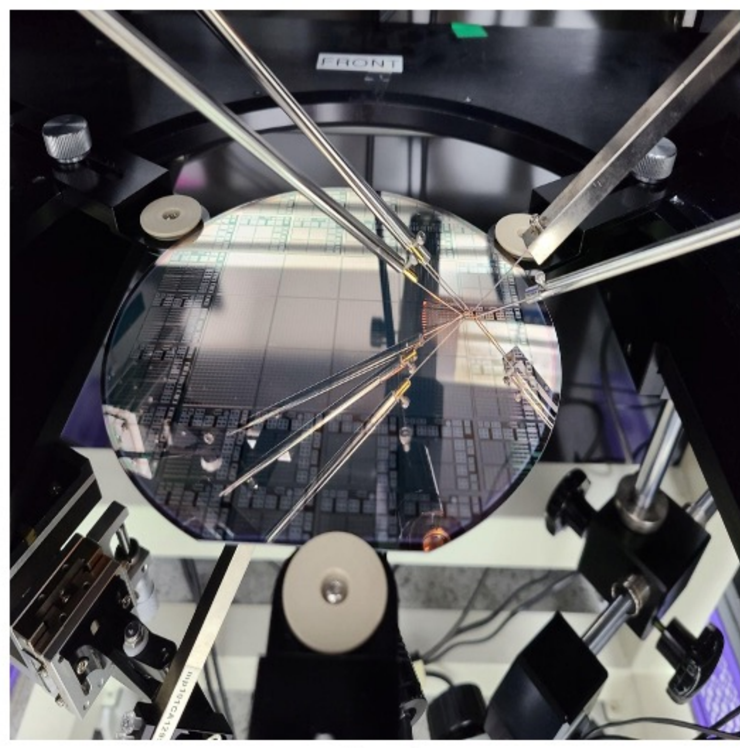

Increased the number of 16X16 arrays from 12 to 21.

Finalized gain layer design to shallow type.

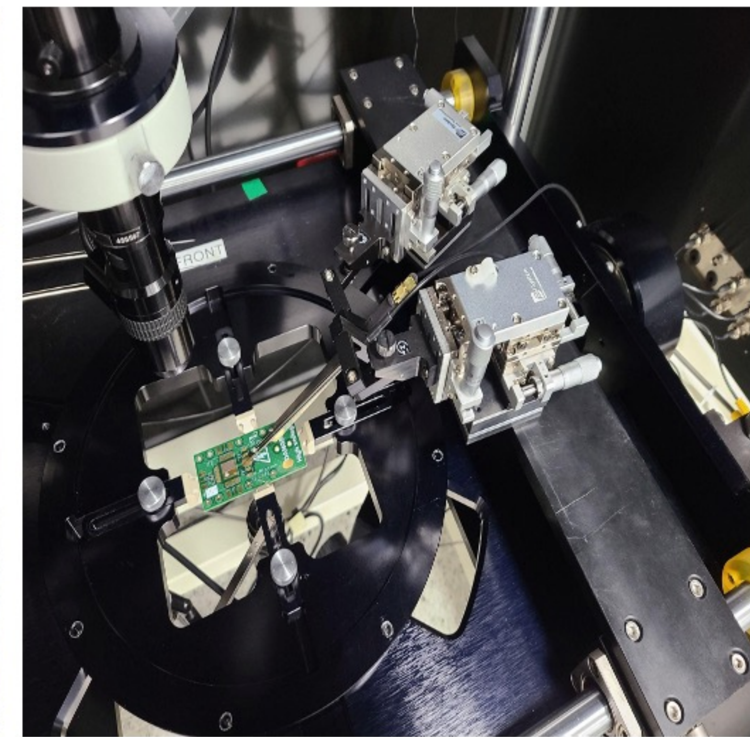
# Probe station setup for wafer-level and sensor-level tests




- Overview




- wafer tray



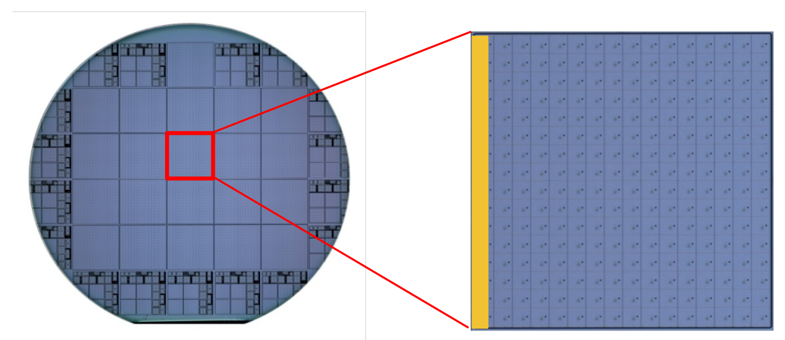

- sensor tray

➢ There are 6 probe arms that use magnets to connect with the station (1 for signal read-out, 1 for bias voltage supplying, and 4 for grounding)

➢ Two types of tray available for wafer-level and sensor-level tests

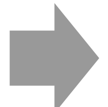
➢ KCMS currently plans to prepare a **probe card** and **switching matrix for 16x16 sensors**

# I-V measurement result of 16X16 array

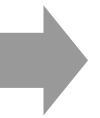


KNU group measured the pad highlighted in yellow box.

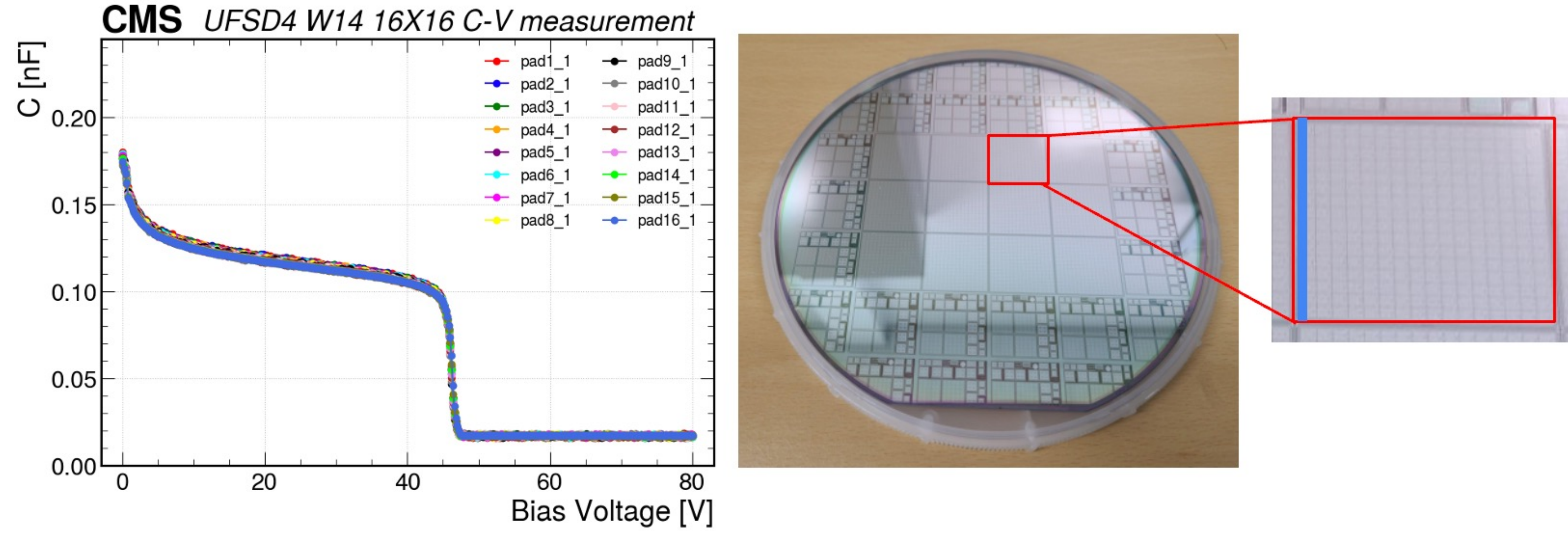
Standard supplier
wafer no.5



new supplier
wafer no.6



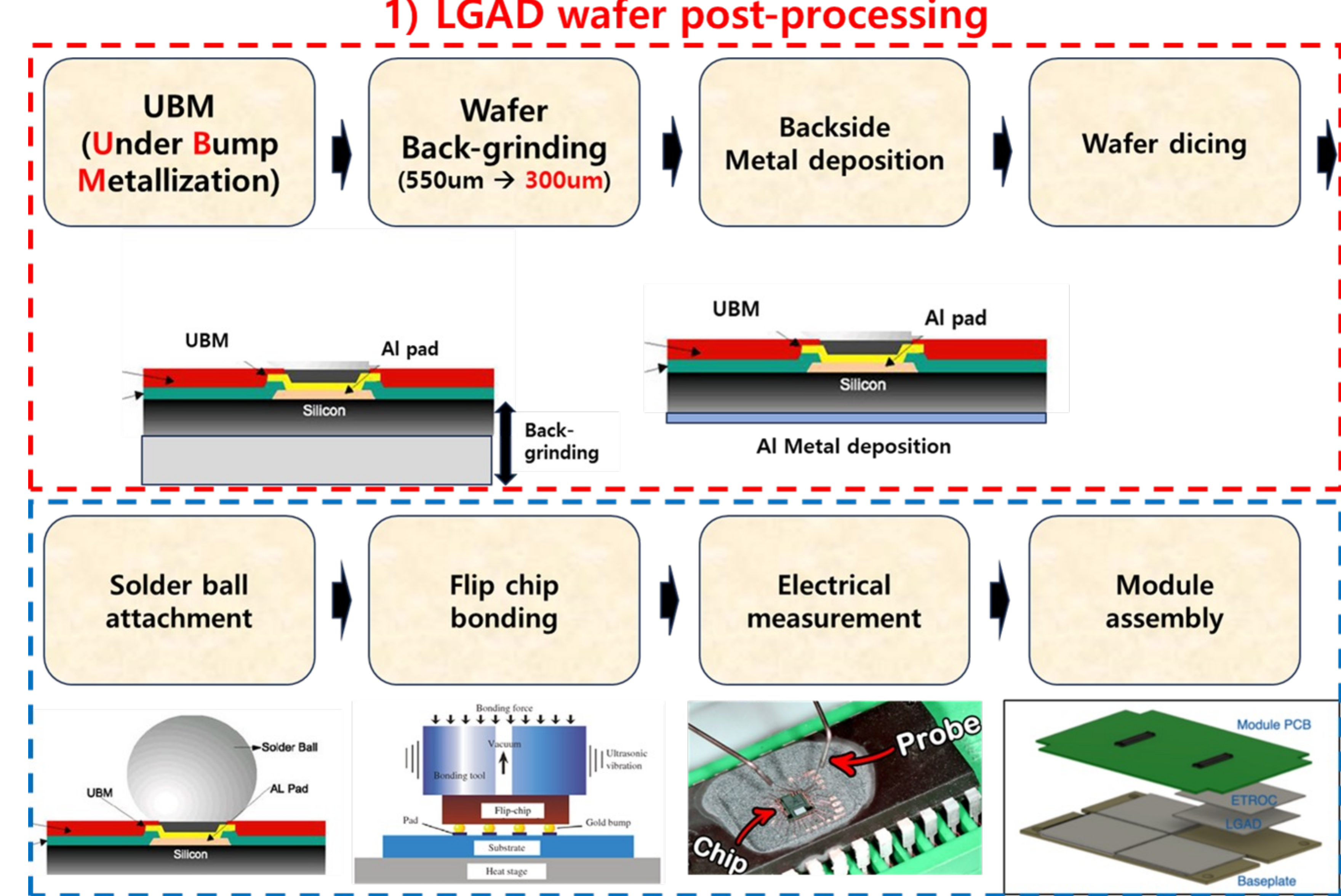
# Gain layer uniformity studies with a column in 16x16 array at KNU




- Measurements performed on 16x16 T10_GR5_STD at KNU to extrapolate the uniformity of the gain layer
- C-V measurement are performed on 16 pads within one column
- Subsequent measurement will be conducted on pads near the center and pads within other reticles

# LGAD wafer post-processing procedure in Korea

LGAD wafer from FBK



# Flip chip bonding test with dummy wafer

- Test Sensors and chips in 6 inch wafer
- 12ea of each type of sensor and chip

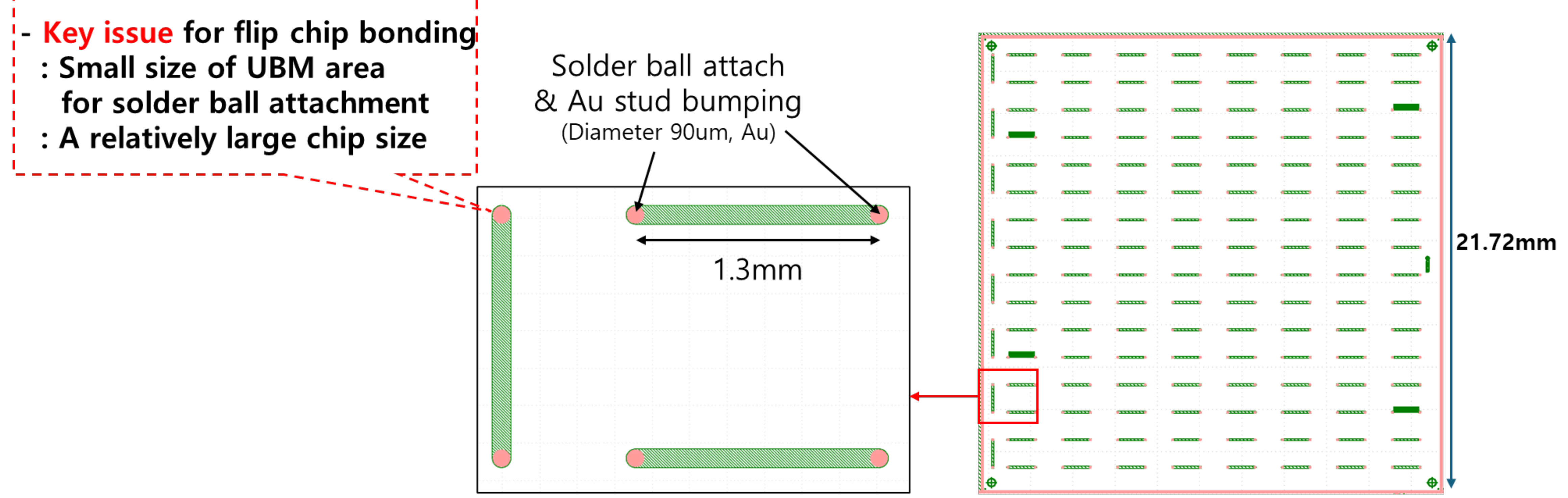
sensor
Bump balls
Low Resistance
High Resistance
ETROC (ROIC part)
Sensor (sensor part)
Au
Au

# Flip chip bonding test with dummy wafer



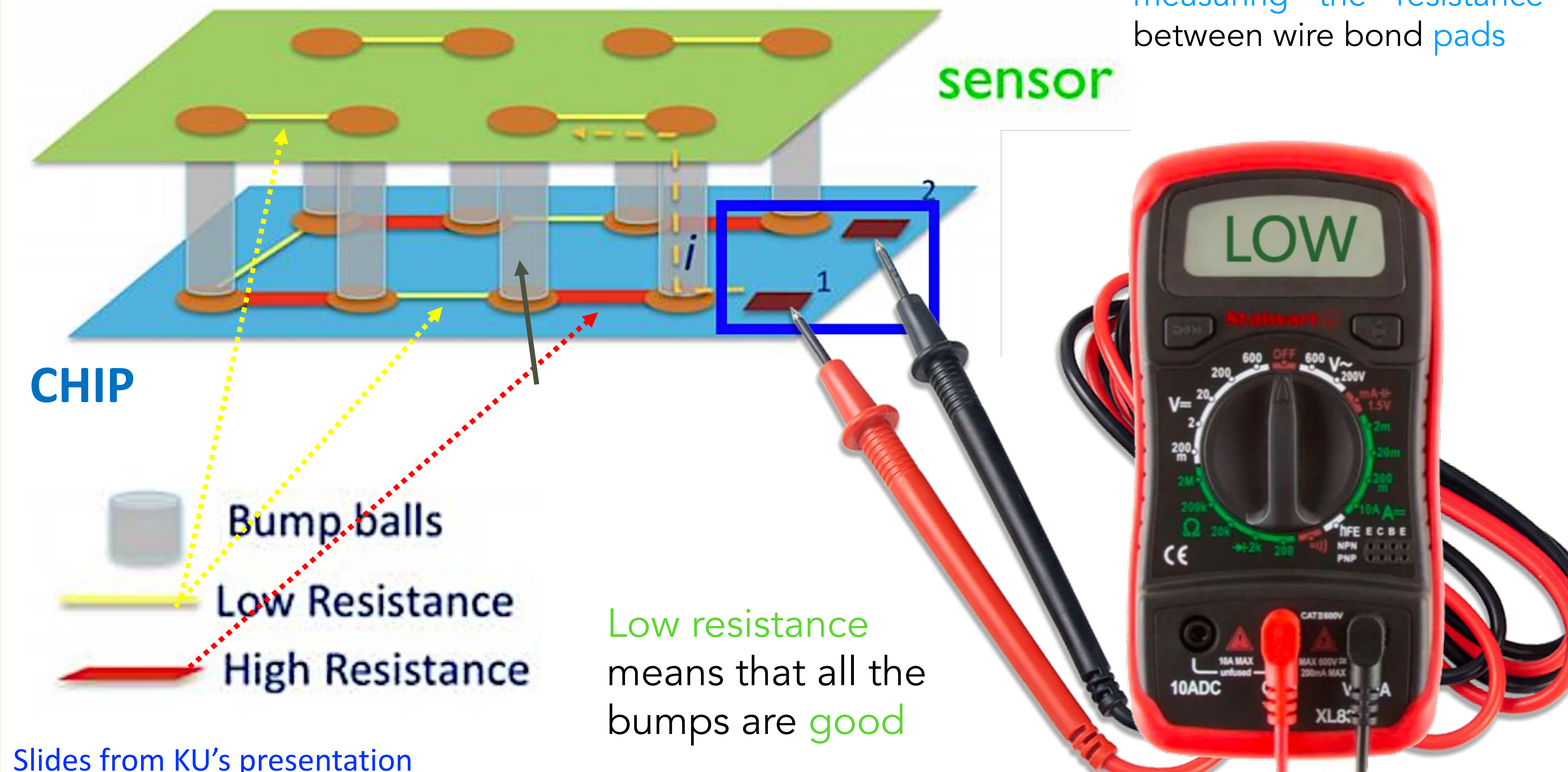
## ❑ Post-processing search and vendor exploration

- Process optimization for flip chip bonding of 16x16 array chip (~22mm x 22mm)
- Vendor searching for stable and cost-effective process



# Concept of electrical tests

determine the number of bumps per serpentine by measuring the resistance between wire bond pads



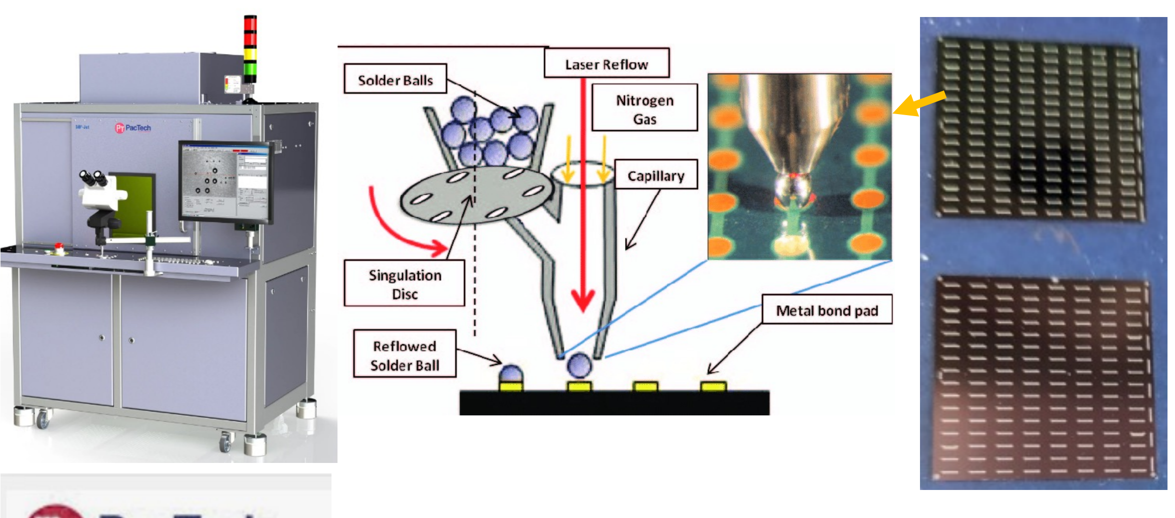

Low resistance means that all the bumps are good

Slides from KU's presentation

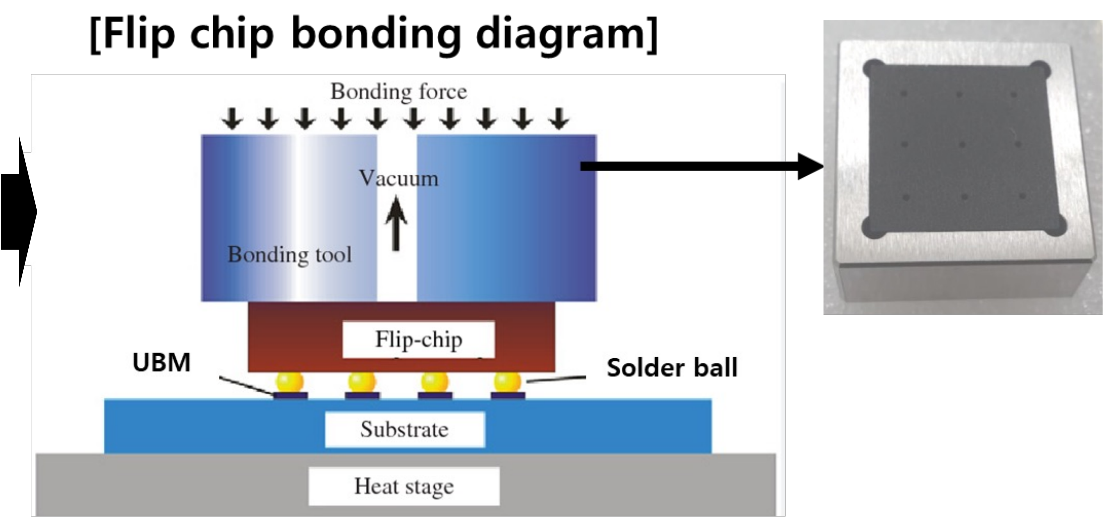
# Flip chip bonding test with dummy wafer

## ❑ Solder ball attachment & Flip-chip bonding process

**[Solder ball of 60um diameter attaching by laser reflow of solder ball]**

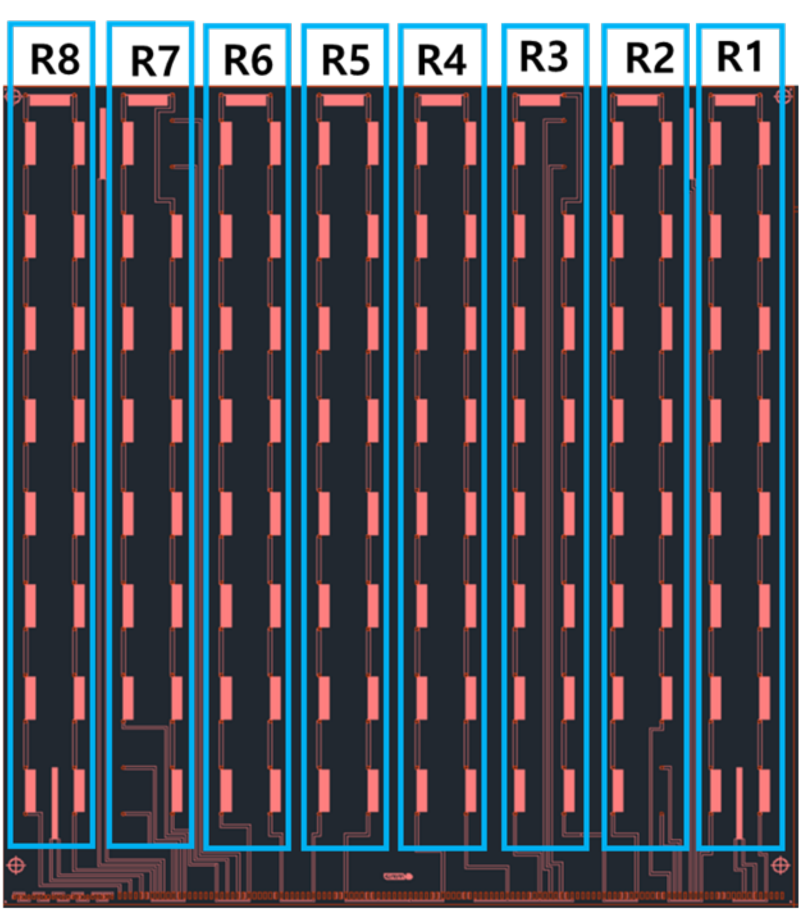



**[Flip chip bonding with customized bonding tool]**



# Flip chip bonding test with dummy wafer

- 1st measurement results of filp-chip bonded sample (2ea)



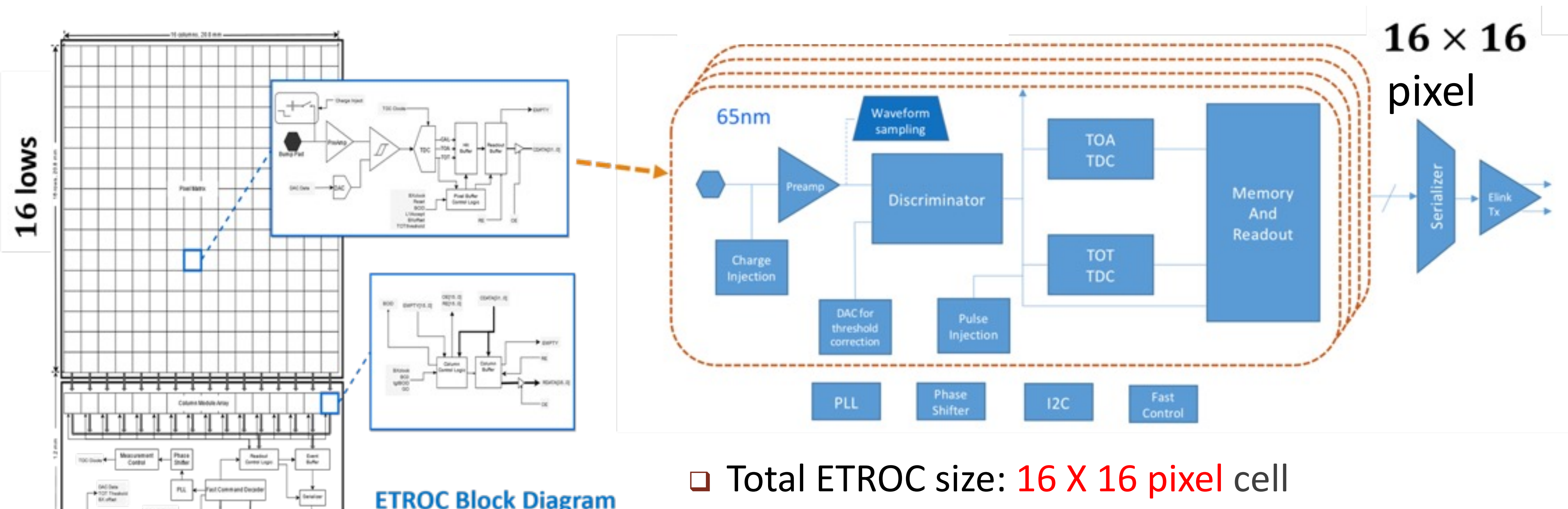
ROIC dummy device

Chip probing for resistance measurement

Unit : Ohm

| Sam-ple | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 |
|---|---|---|---|---|---|---|---|---|
| S1 | 808 | 276 | 253 | 185 | 20 | 21 | 215 | 516 |
| S2 | 291 | 33 | 37 | 202 | 57 | 27 | 240 | 440 |

# Endcap Timing Layer ReadOut Chip (ETROC)



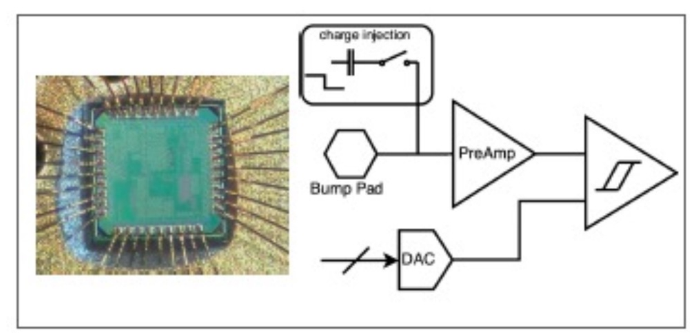

ETROC Block Diagram

- Total ETROC size: 16 X 16 pixel cell
  - One pixel cell size: 1.3mm X 1.3mm to match the LGAD sensor pixel size
- Targeting signal charge (1MIP): 6 - 20 fC
- TDC (time-to-digital converter) range
  - ~5 ns TOA (time of arrival)
  - ~10 ns TOT (time over threshold)

CHANG-SEONG MOON (KNU)

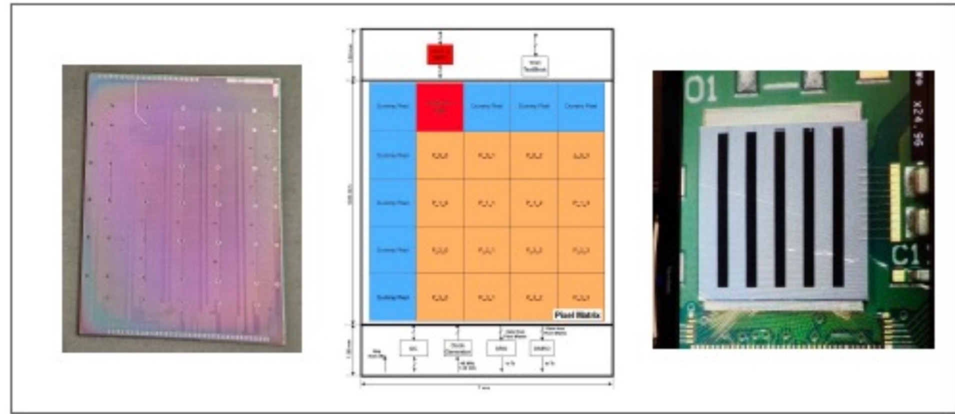
# ETROC Development Plan

## 2018
### ETROC0 (1x1)




- Analog front-end only
- Wire-bonded with LGAD sensor reached ~33 ps time resolution per hit with preamp. waveforms
- Passed 100 Mrad TID

## 2020
### ETROC1 (4x4)



- Added low-power TDC and 4x4 H-tree for clock distribution
- Bump-bonded with LGAD sensor reached ~42 ps time resolution per hit with TDC data

## 2023
### ETROC2 (16x16)

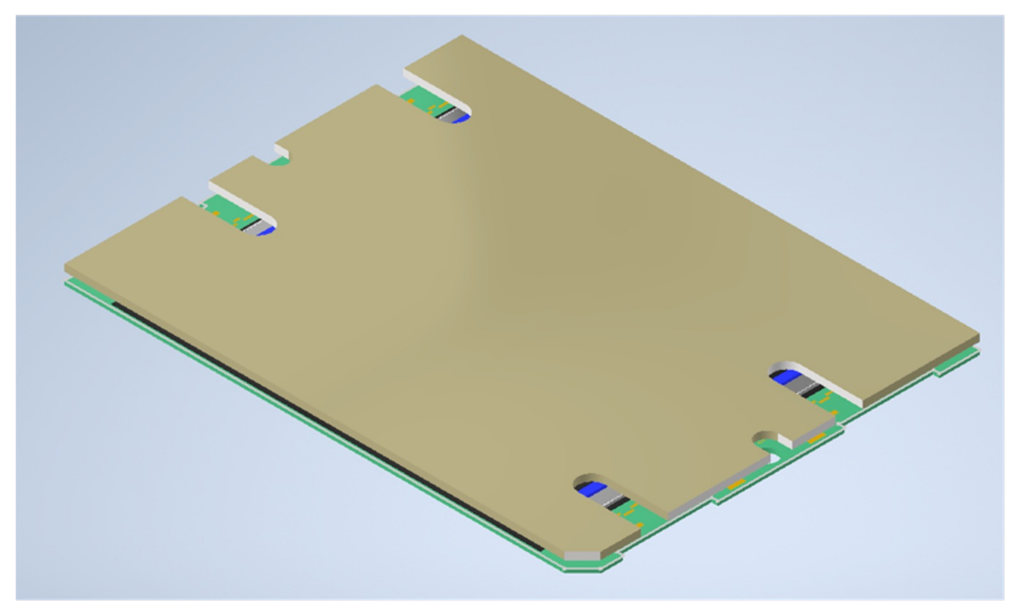
- First full-size chip (16x16) with all desired functionalities included
- All analog blocks silicon-proven; all digital blocks were verified in FPGA emulator

## ❑ ETROC3 : Final chip

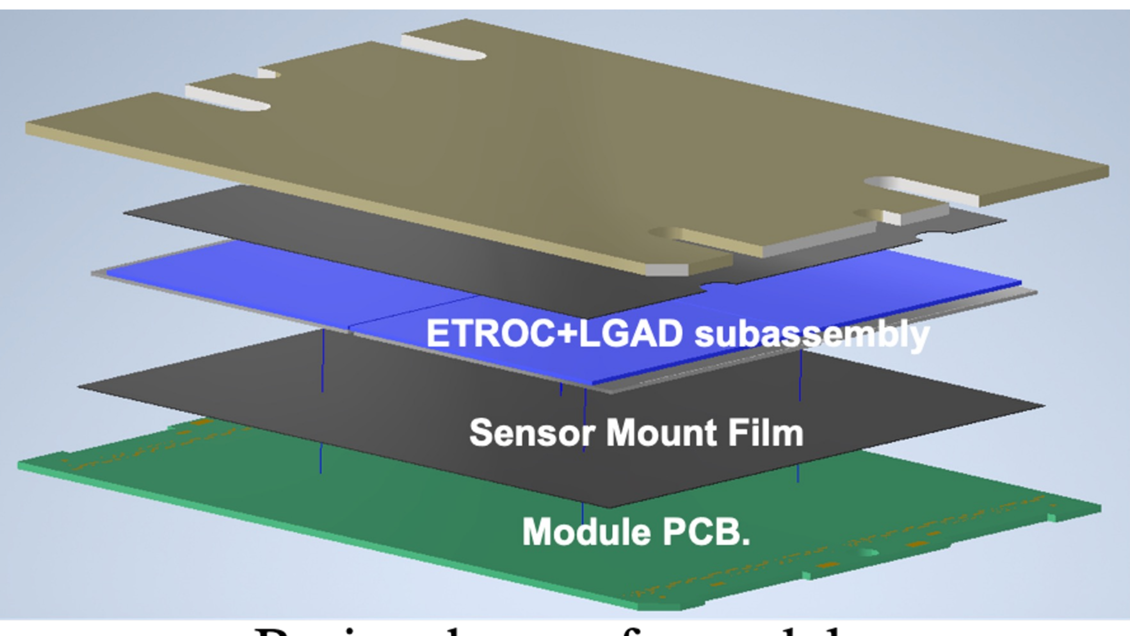
- The same functionalities as ETROC2, with improvements based on what will be learned from extensive ETROC2 testing
- Submission scheduled for 2024

# ETL Module design overview

## ❑ Module design overview



PCB + subassembly




Basic scheme of a module

## ❑ Module PCB

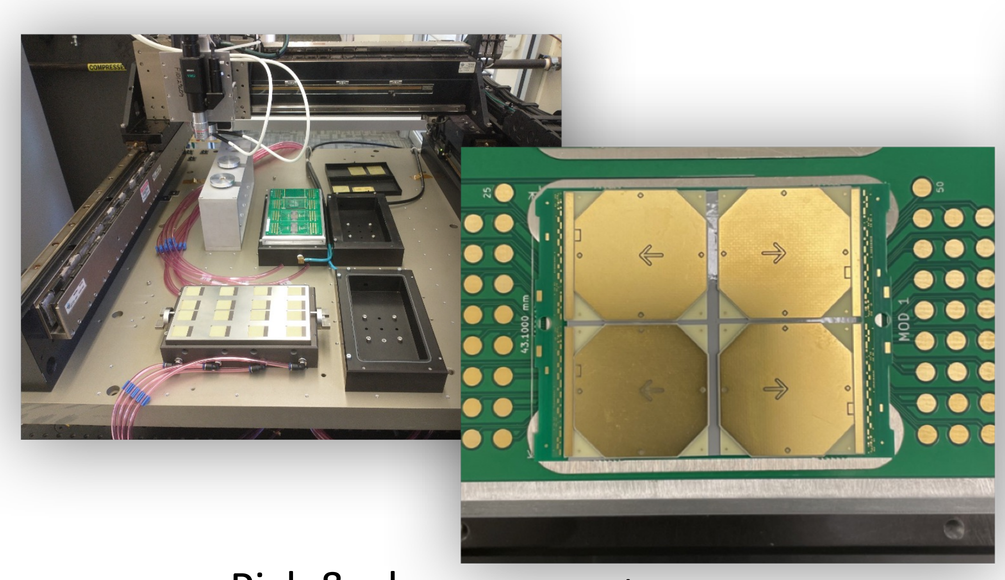
- Printed circuit board that serves as the power and readout interface for the module

## ❑ 4x ETROC+LGAD subassembly

- 2x2 arrangement of bump-bonded assemblies
- Each of a 16x16 pixel LGAD sensor and an “ETROC” readout chip

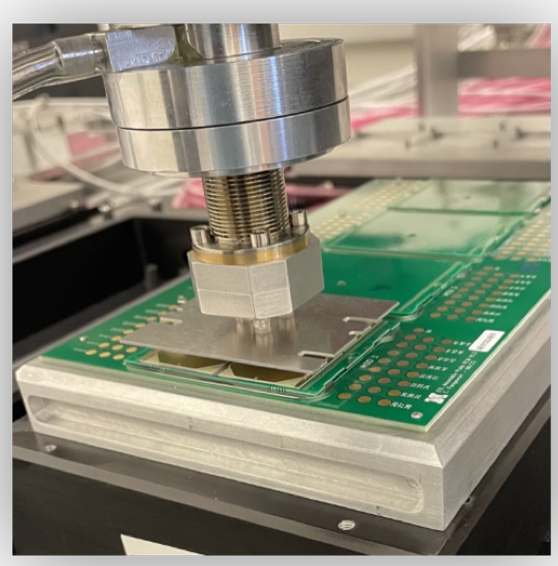
# Assembling the ETL Modules

- The ETL detector will need ~8 thousand modules
- Each module will be made of 4 LGAD sensors and ETROCs
- An automated robotic gantry will be used for precision placement at the 10 micron level
- All modules will then be assembled into disks at CERN




Pick & place sensor + PCB

Wirebond and encapsulating



Apply film to baseplate, pick and place, and cure film

# KCMS contribution for MIP Timing Detector (MTD)

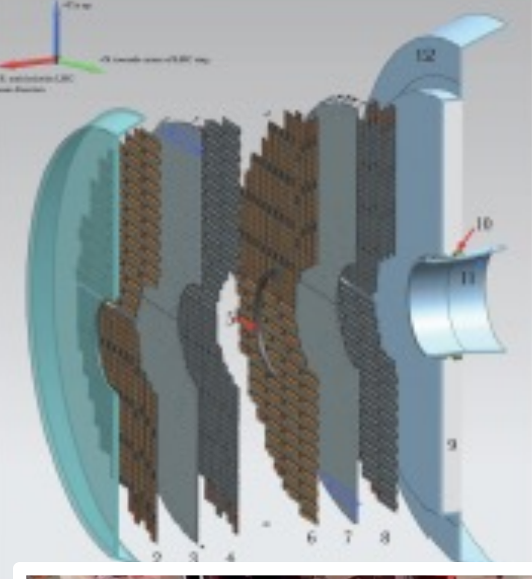
Mitigate the pileup effects at HL-LHC using precision timing information to enhance and expand the physics reach our detector performance.

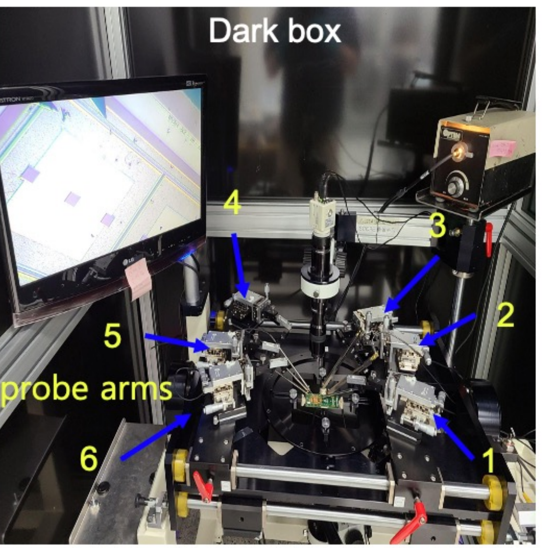
**Main contributions from KCMS**

- Low Gain Avalanche Detector (LGAD) sensor development & production
- LGAD & ETROC Bump-Bonding development & processing
- ETL (Endcap Timing Layer) Module Assembly development & production

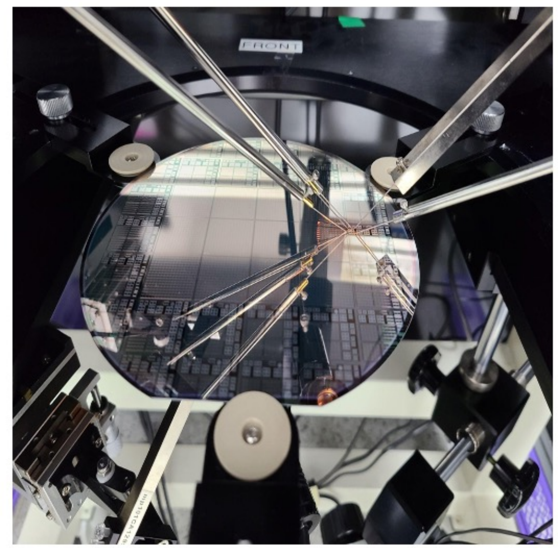
**KCMS contribution for MTD : 2.2 MCHF (25% of the total endcap coverage)**

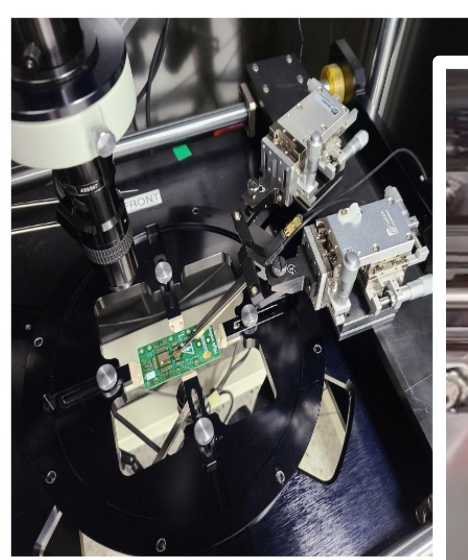
**Total contribution with MTD on the Phase 2 will be ~6 MCHF**

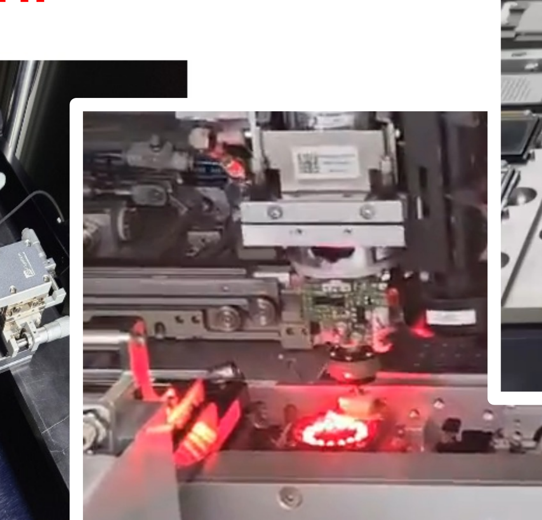


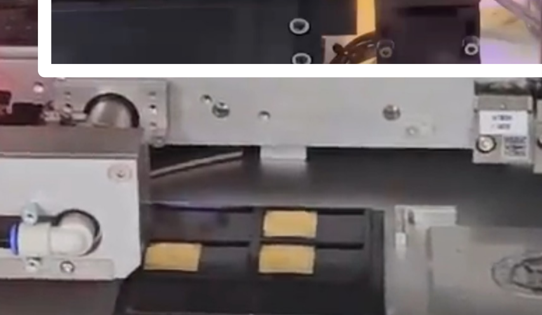


• Overview

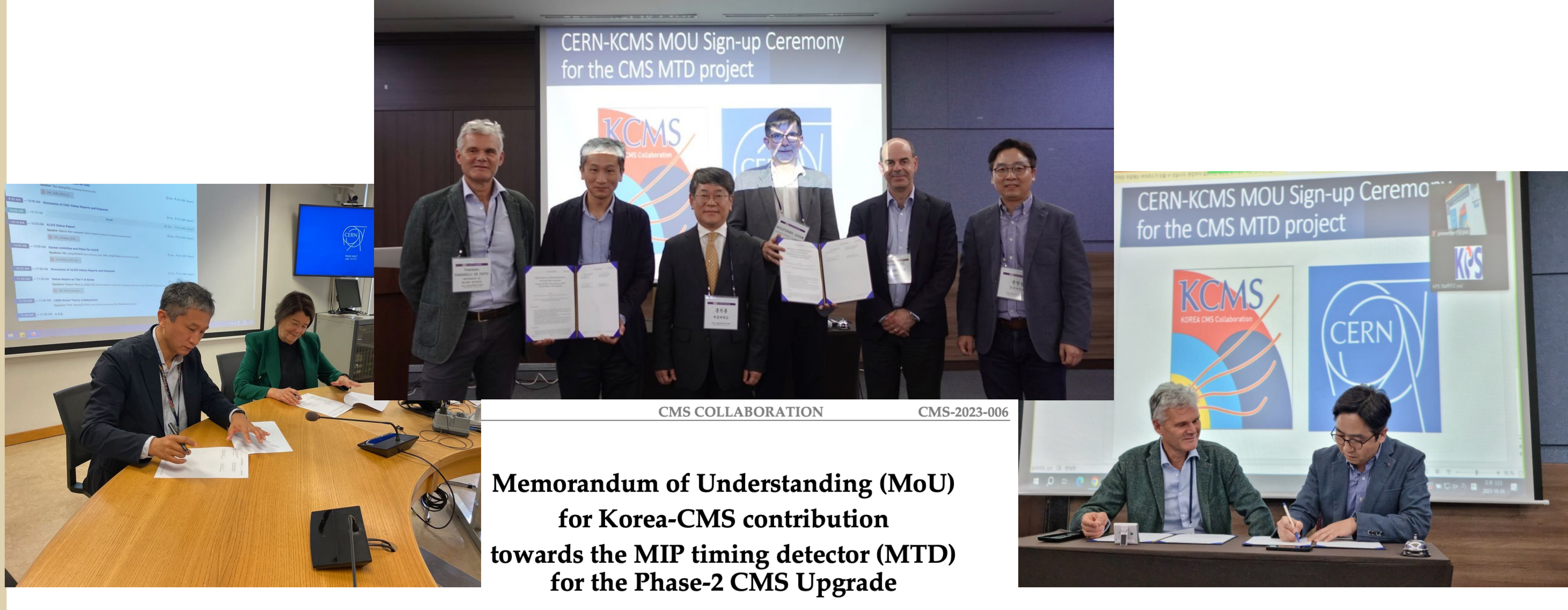

• wafer tray


• sensor tray





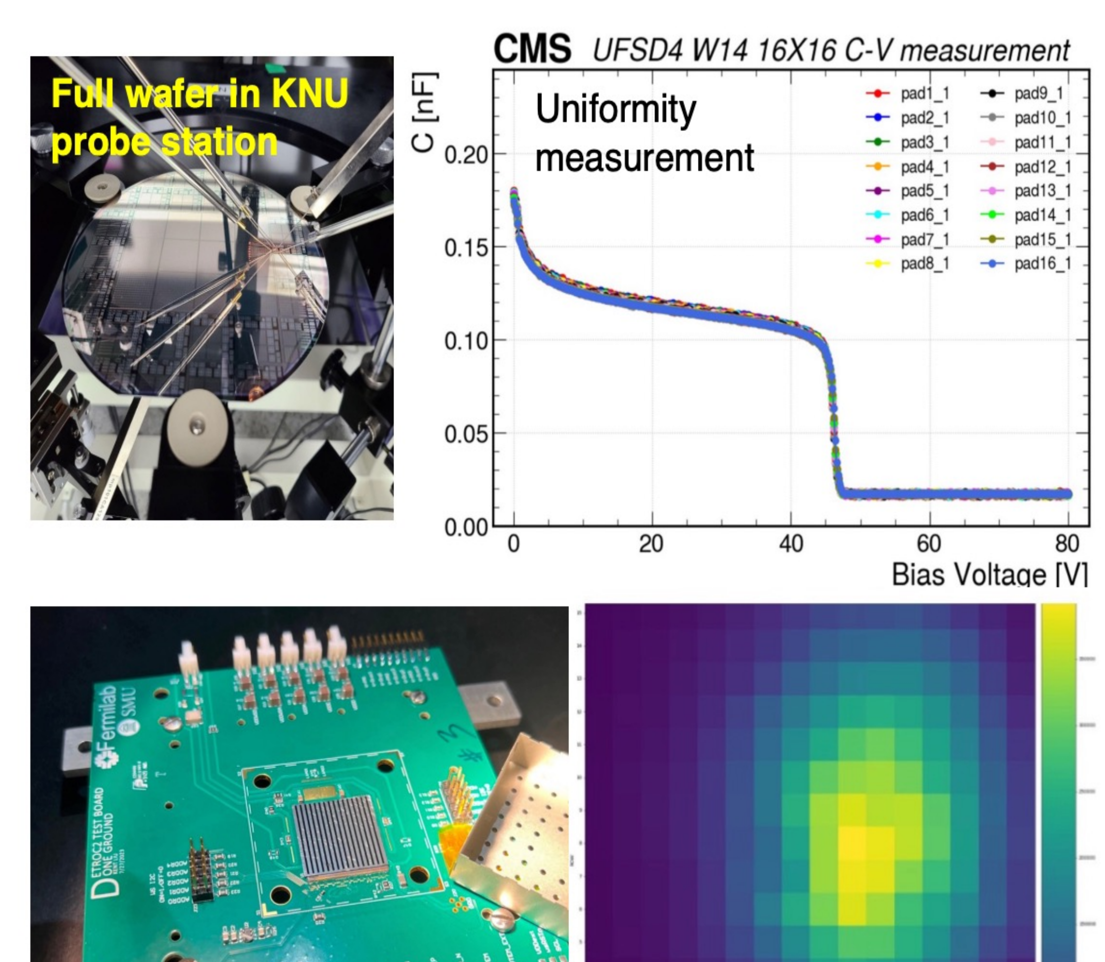
# CERN-Korea CMS Sign-up Ceremony for the MTD project




- ❑ **Korea CMS group** will contribute the **LGAD production (25%), bump bonding process, front-end ASICs and module structures**, etc.
- ❑ Total budget: **2.2M CHF** supported by National Research Foundation of Korea (NRF)

# Current Korea CMS Activities and Future plan

- **KCMS responsible for the delivery of one layer of ETL sensors!**
  - **25% of the total endcap coverage**
- **Significant contributions to prototyping towards production:**
  - **LGADs prototyping and validation:**
    - Detailed testing of prototype LGADs informed vendor qualification
    - Probe station measurements to verify quality and uniformity of full-size wafers
  - **ETROC2 testing**
    - Active in ETROC testing, including test beam campaigns for validation of the performance of the LGADs + ETROC chain
  - **Wafer processing:**
    - Exploring wafer processing with one of the qualified LGADs vendors for wafer thinning, dicing, and surface preparation at Korean companies for the production phase
  - **Bump-bonding:**
    - Exploring options with Korean companies for LGAD-to-ETROC bump-bonding during production



# Summary

- The CMS MIP Timing Detector will measure precision timing of charged particles produced inside CMS.
  - Provides significant pileup mitigation, furthering the experiment's mission in the HL-LHC era.
  - Brings new capabilities to CMS that could help to search new phenomena in the HL-LHC.
- BTL will be instrumented with LYSO crystals + SiPMs, read-out by the TOFHIR
  - Beginning of life performance (30-40 ps) within requirements
  - End-of-life performance (~ 60 ps) close to requirements
  - The BTL prototyping phase is completed and now entering production phase
- ETL will be instrumented with LGADs read out by the ETROC
  - Performance at beginning and end of life within requirements (single hit resolution < 50 ps)
  - LGAD market survey done → Will enter a tender process soon.
  - Full-scale 16x16 ETROC2 arrived and Initial system test with bare ETROC2 in progress.
- KCMS contribution for MTD : 2.2 MCHF (25% of the total endcap coverage)
  - Low Gain Avalanche Detector (LGAD) sensor development & production
  - LGAD & ETROC Bump-Bonding development & processing
  - ETL (Endcap Timing Layer) Module Assembly development & production