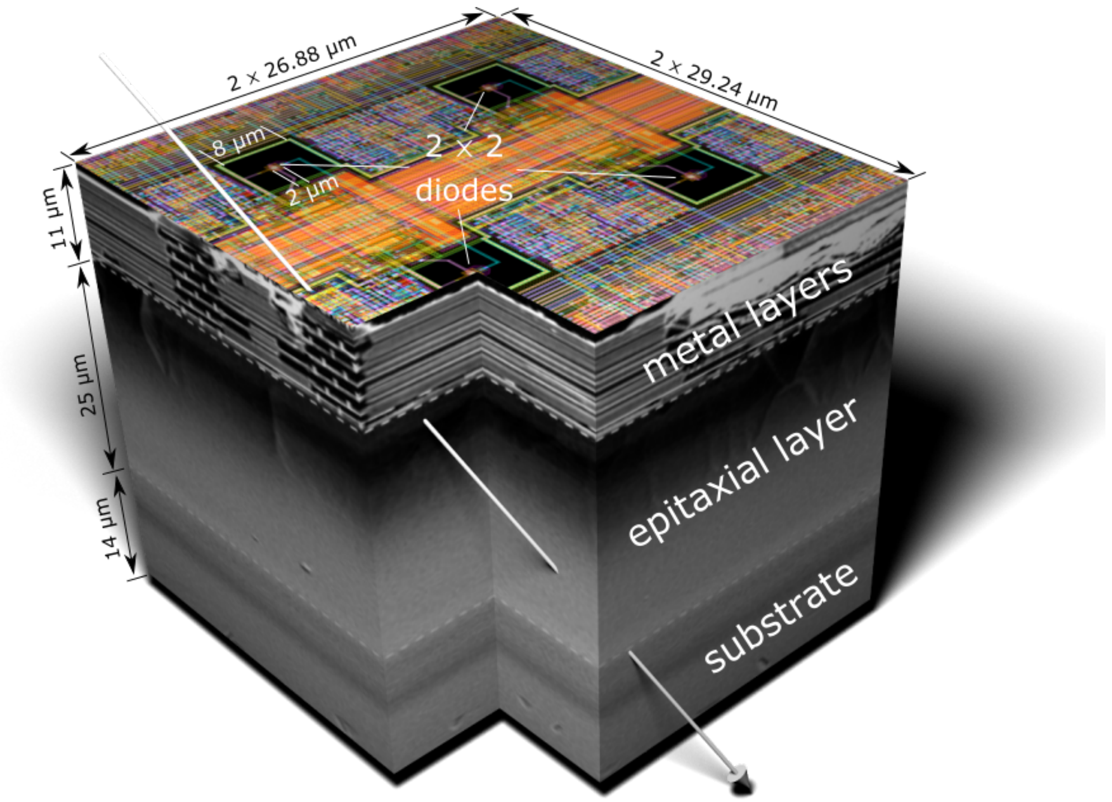
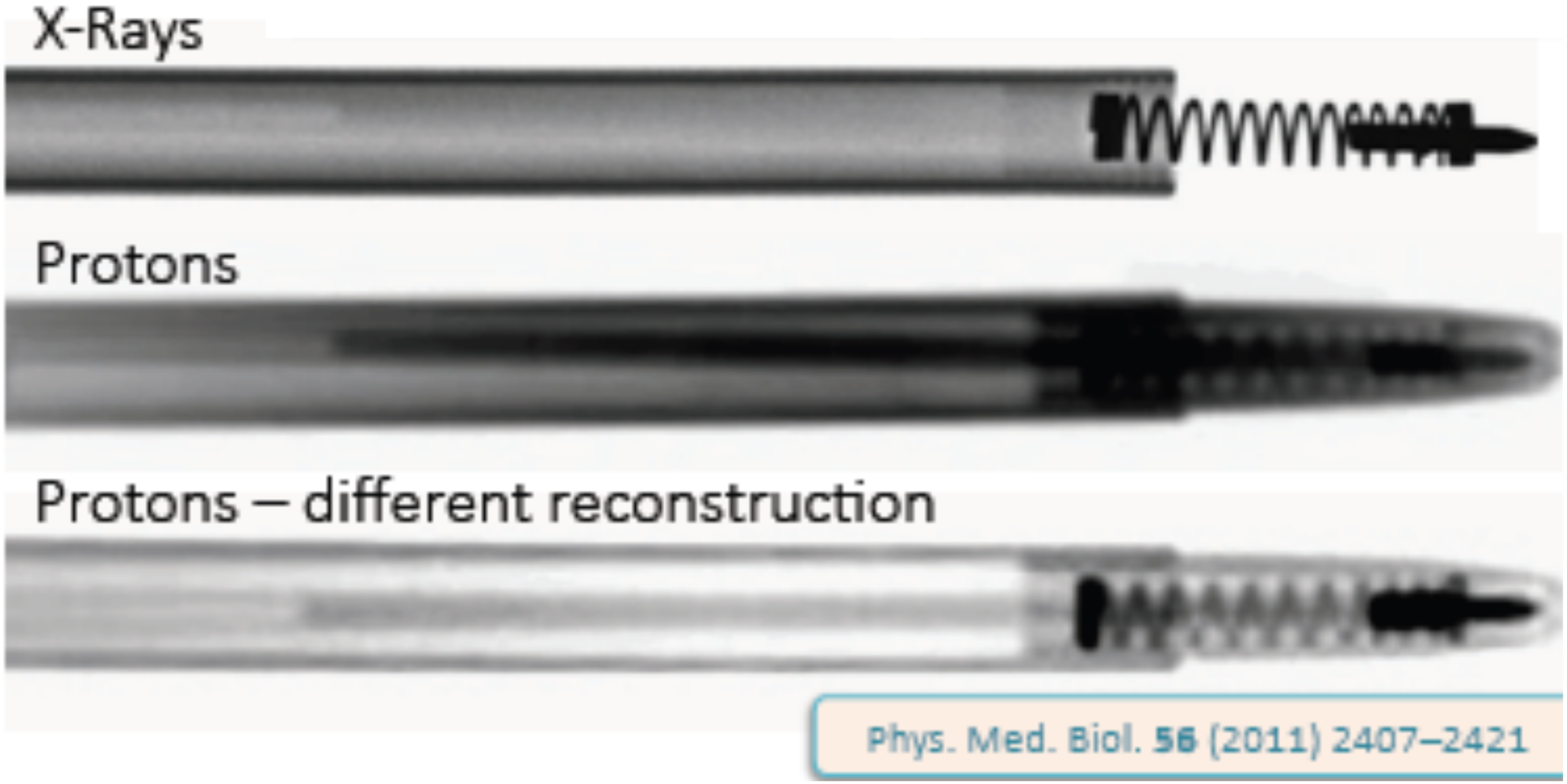
Silicon Detector Overview, Application and Outlook



In-Kwon Yoo (Physics, Pusan Nat'l University)

On behalf of Luciano Musa (CERN)

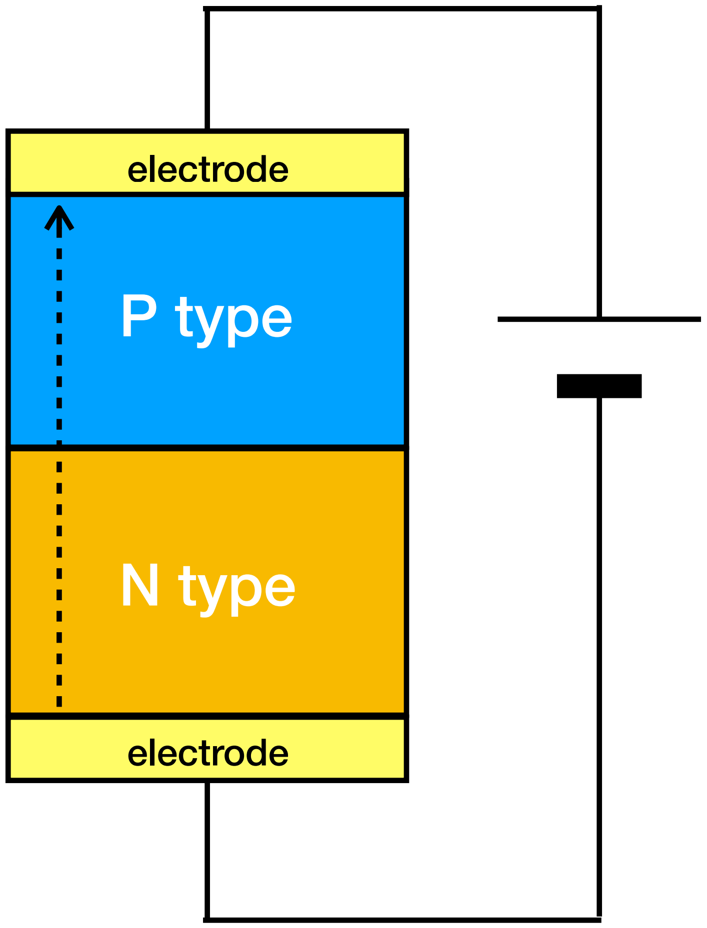
How can we look into?



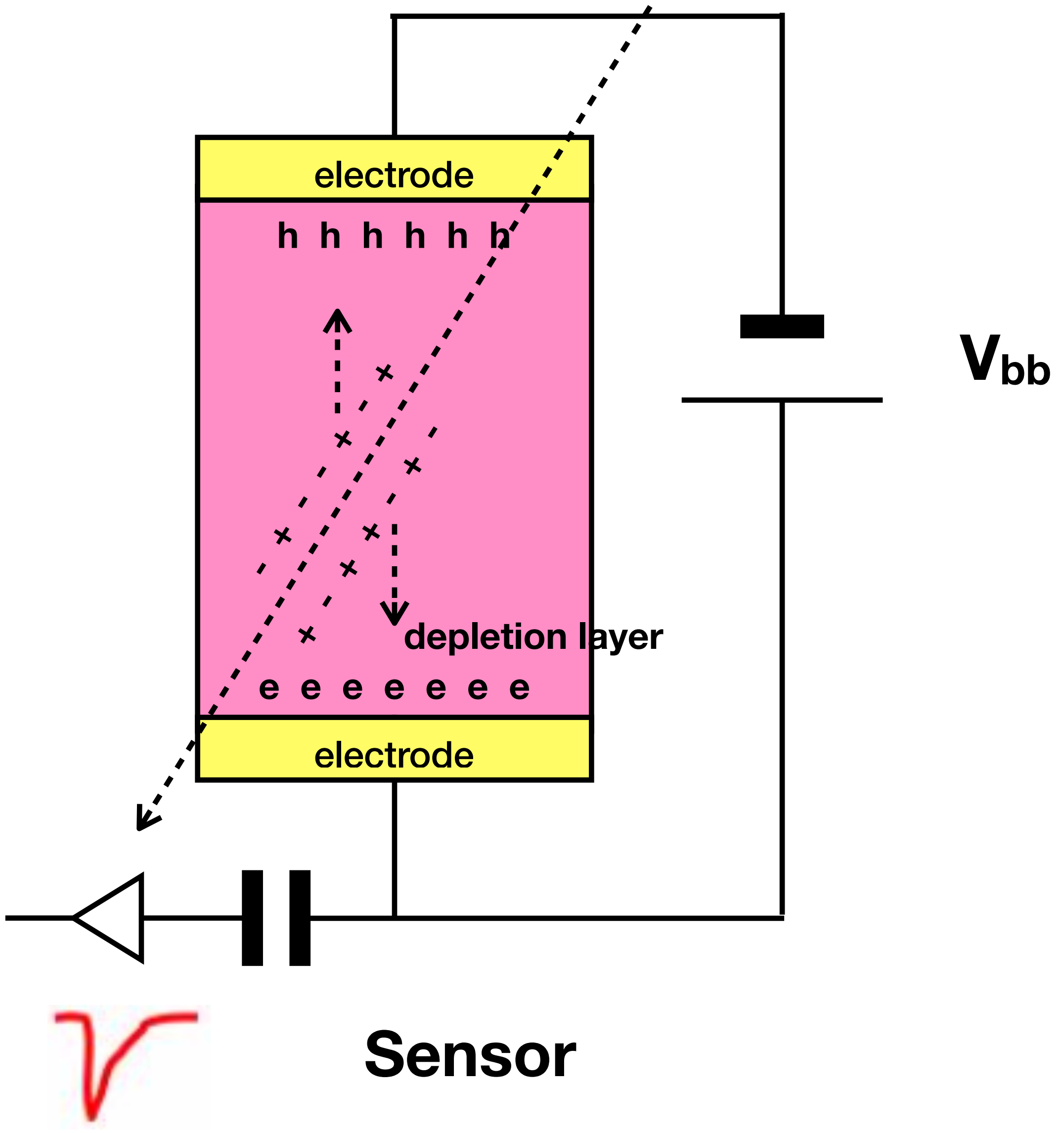
Phys. Med. Biol. 56 (2011) 2407–2421

- What probe? … interaction resolution
- How to detect … space-time resolution

Principle of Silicon Detector



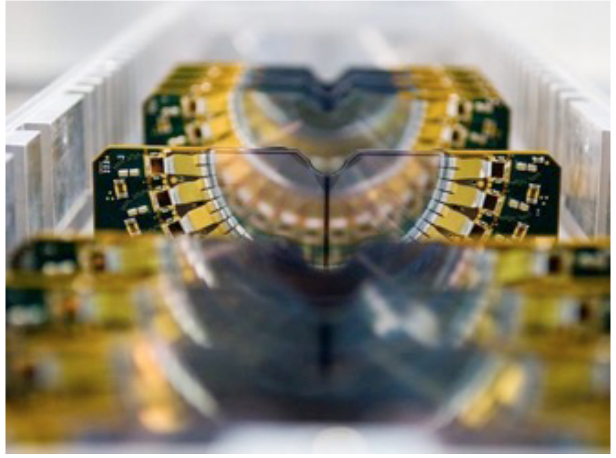
Diode



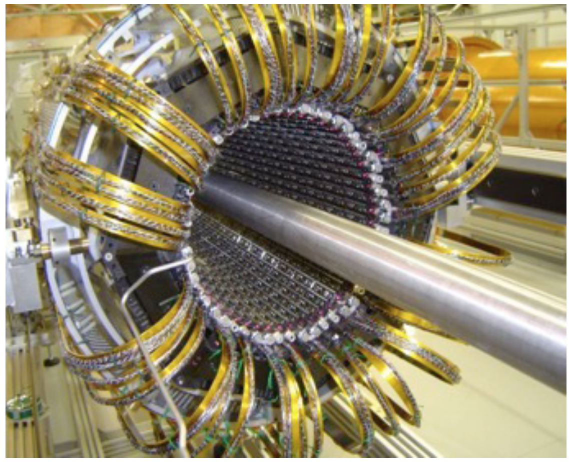
Sensor

Silicon Detectors in HEP

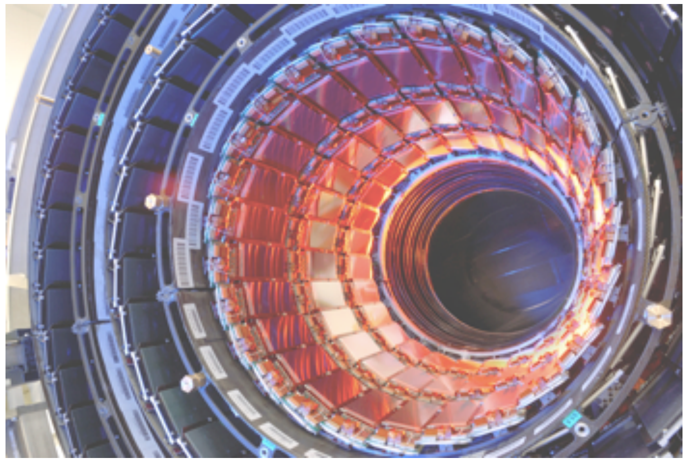
ALICE Pixel Detector



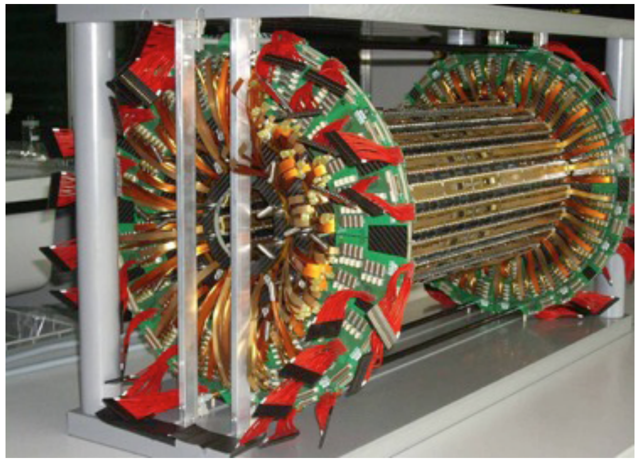
LHCb VELO



ATLAS Pixel Detector



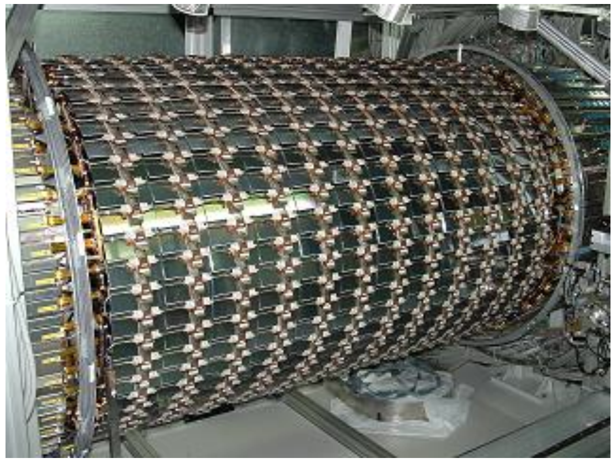
CMS Strip Tracker IB



CMS Pixel Detector

ALICE Drift Detector

ALICE Strip Detector



ATLAS SCL Barrel

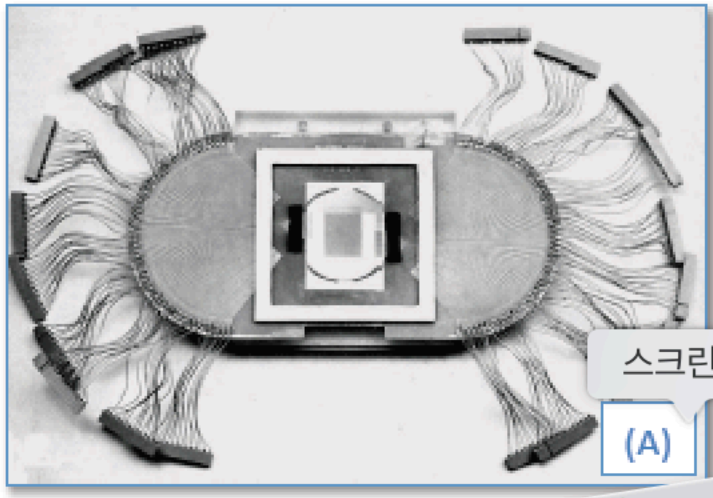
Brief History

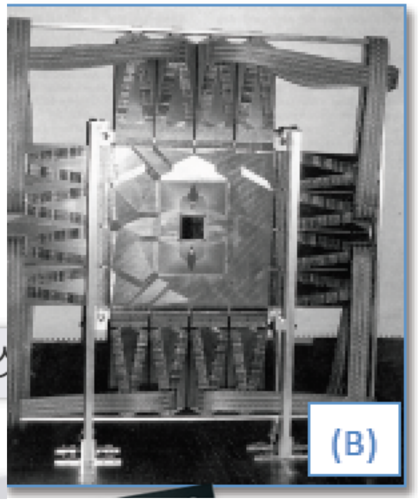
J. Kemmer, et al., “Development of 10-micrometer resolution silicon counters for charm signature observation with the ACCMOR spectrometer”, Proceedings of Silicon Detectors for High Energy Physics, Nucl. Instr. and Meth. 169 (**1980**) 499.

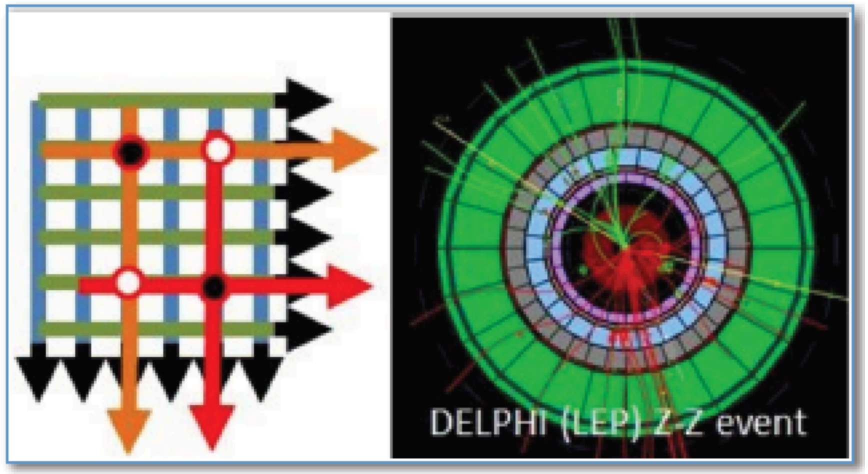
First use of silicon strips detectors by NA11(CERN SPS) and E706 (FNAL)
(A) NA11 (**1981**): 6 planes (24 x 36mm2): resistivity 2-3 kΩcm, thickness 280µm, pitch 20µm
(B) E706 (**1982**): 4 planes (3x3 cm2) + 2 planes (5x5cm2)

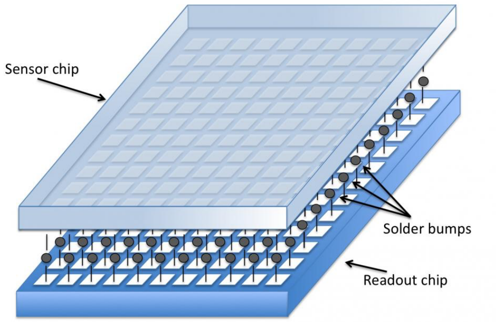
1990s - LEP, first silicon vertex detectors installed in DELPHI and ALEPH experiments, then OPAL and L3
1989 - first DELPHI vertex detector, consisting of two layers of single-sided strip detectors

1995 – First Hybrid Pixel detector installed in WA97 (CERN, Omega facility)
1996/97 – First Collider Hybrid Pixel Detector installed in DELPHI (CERN, LEP)



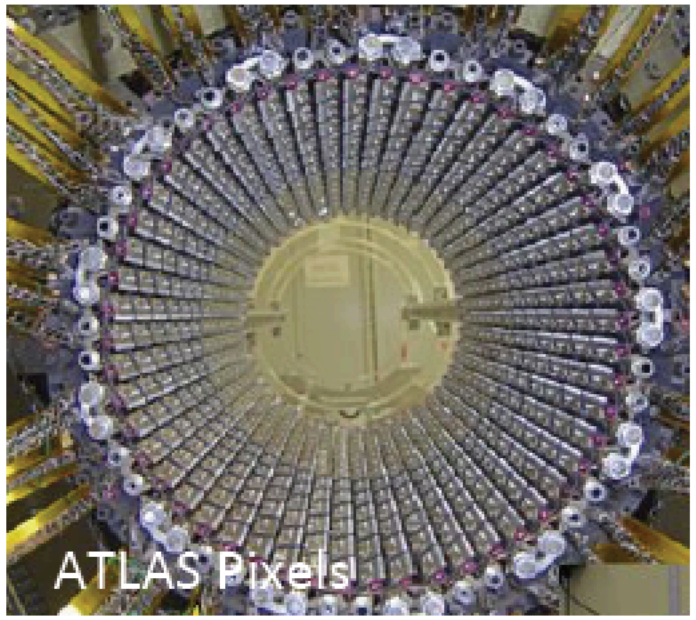


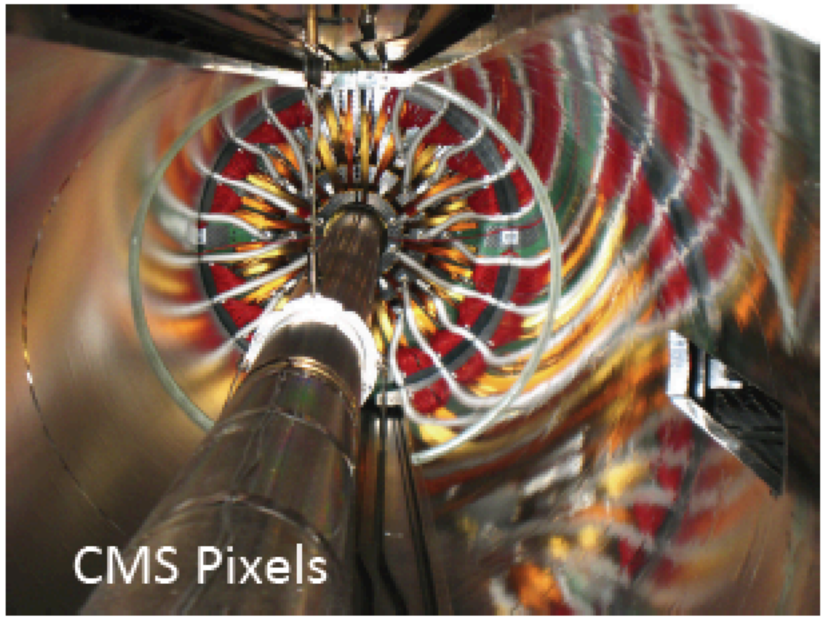


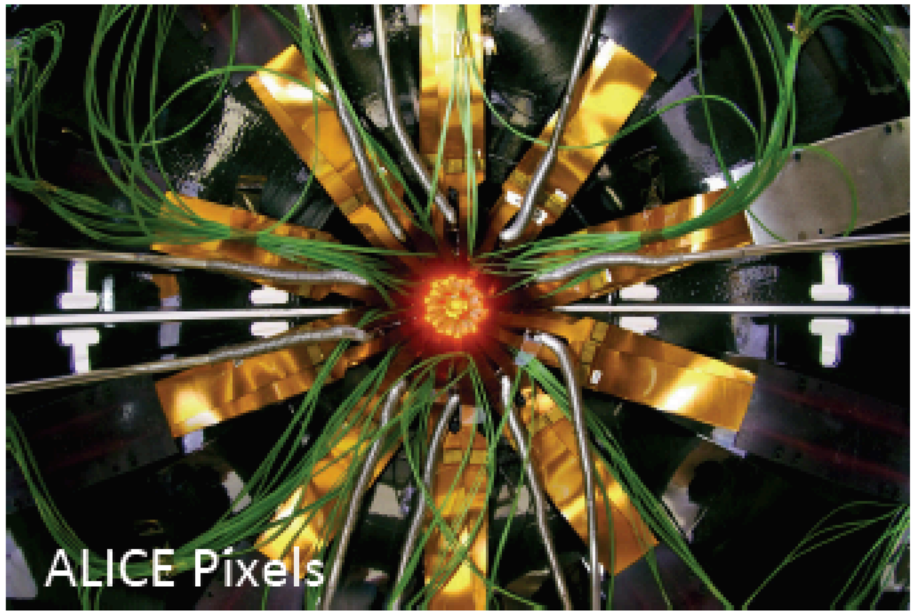


Pixel Detectors at LHC experiments

KoALICE





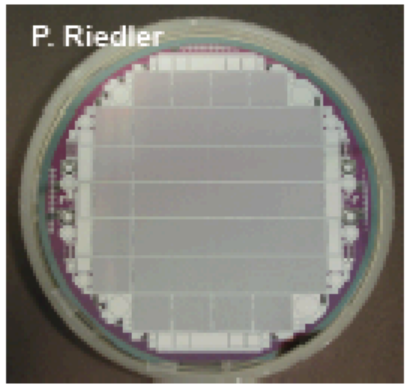


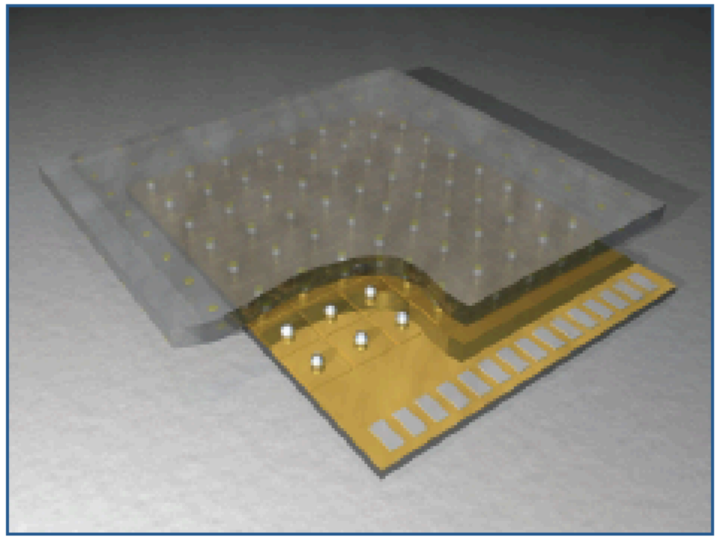
- 10 yrs later …

Parameters	**ALICE**	**ATLAS**	**CMS**
Nr. layers	2	3	3
Radial coverage [mm]	**39** - 76	**50** - 120	**44** – 102
Nr of pixels	9.8 M	80 M	66 M
Surface [m^2]	0.21	1.7	1
Cell size (rϕ x z) [μm^2]	50 x 425	50 x 400	100 x 150
Silicon thickness (sens. + ASIC) - x/X_0 [%]	0.21 + 0.16	0.27 + 0.19	0.30 + 0.19

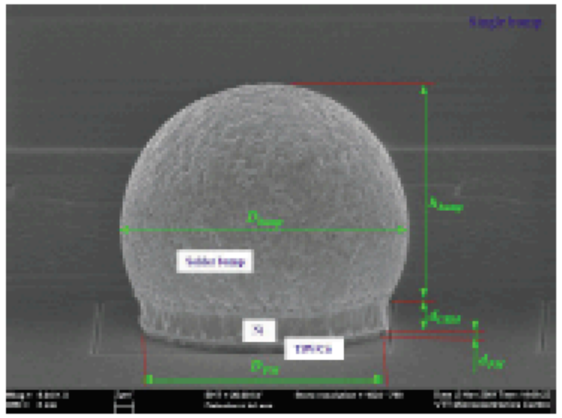
Technology

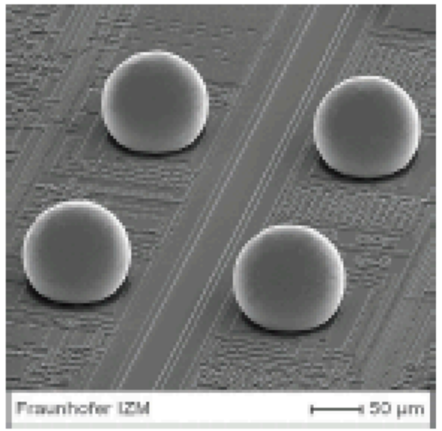
- Limited number of sensors producers (~10 world-wide)
- no industrial scale production ➔ high cost


P. Riedler


Azom.com

- Complex and costly interconnection between sensors and ASIC
- Interconnection technology (micro-bump bonding) limits:
  - pitch (currently ~30µm)
  - input capacitance ➔ power


VTT Microelectronics Centre



Fraunhofer IZM

Lower production cost

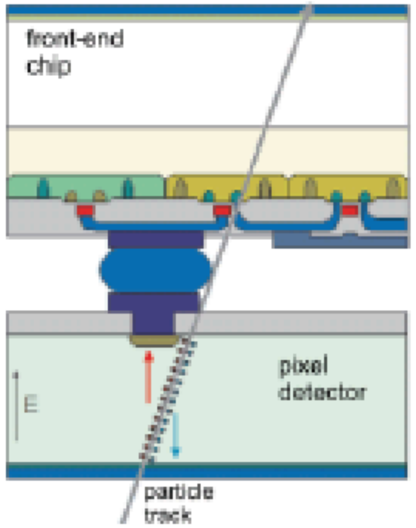
Higher integration (pitch, x/X_0)

Lower power (x/X_0, cost)

➔ CMOS Pixel Sensors

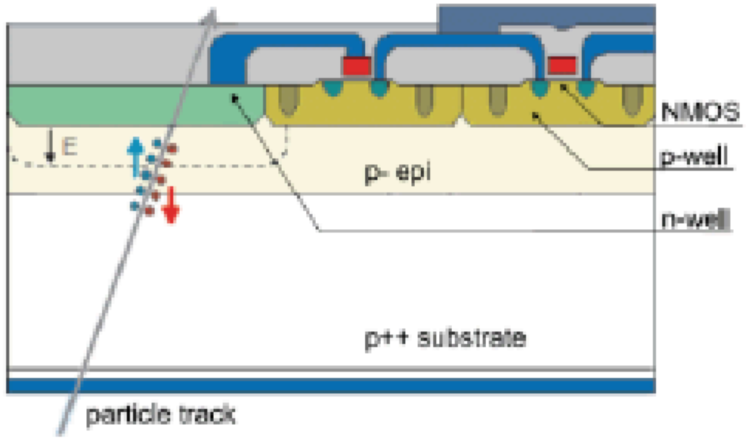
MAPS Technology

Hybrid Pixel Detector



N. Wermes (Univ. of Bonn)

Monolithic Pixel Detector



N. Wermes (Univ. of Bonn)

Since the very beginning of pixel development (CERN RD 19):

dream to integrate sensor and readout electronics in one chip

Motivation to reduce: cost, power, material budget, assembly and integration complexity

Several major obstacles to overcome:

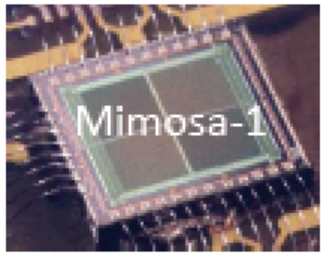
- CMOS generally not available on high resistivity silicon (needed as bulk material for the sensor) ✓
- Full CMOS circuitry not possible within the pixel area (only one type of transistor ➔ slow readout) ✓

Exist in many different flavours: **CMOS**, HV CMOS, DEPFET, SOI

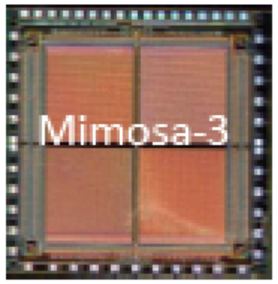
The following will cover only CMOS Active Pixel Sensors (CMOS MAPS) **= CMOS Active Pixel Sensors (CPS)**

MAPS Detectors

Owing to the industrial development of CMOS imaging sensors and the intensive R&D work (IPHC, RAL, CERN)



1999



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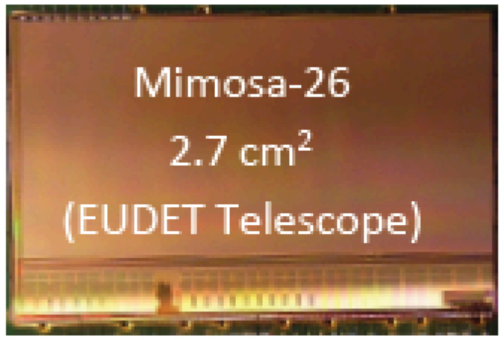
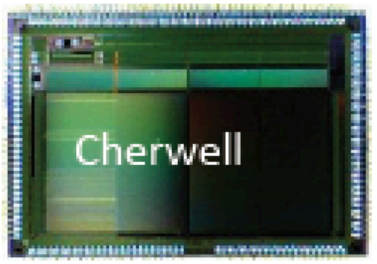
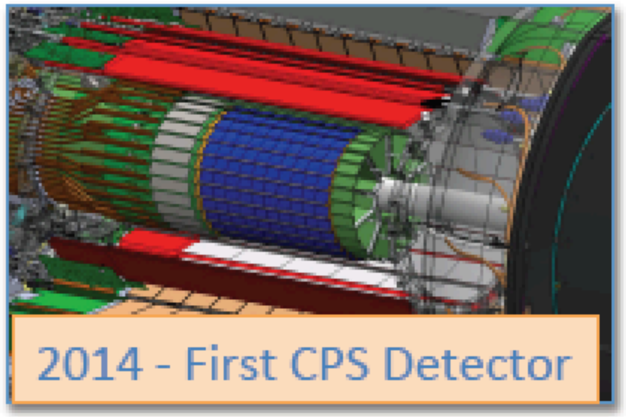




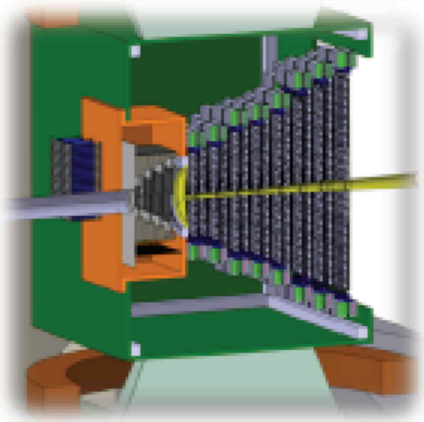
2016

… several HI experiments have selected CMOS pixel sensors for their inner trackers

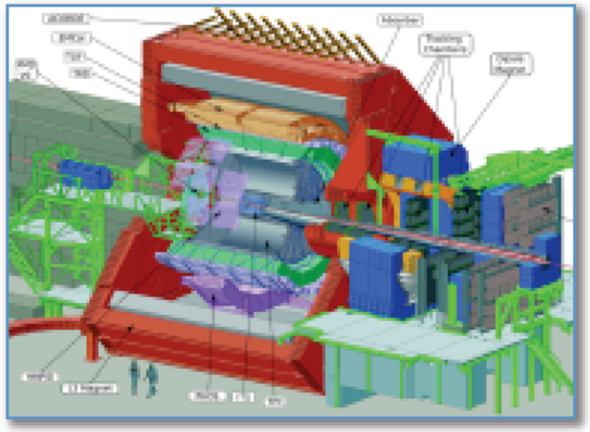


2014 - First CPS Detector

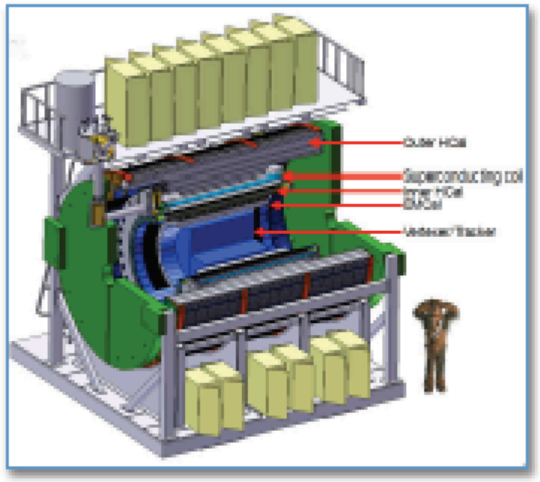
STAR HFT
$0.16\ \text{m}^2$ – 356 M pixels



CBM MVD
$0.08\ \text{m}^2$ – 146 M pixel



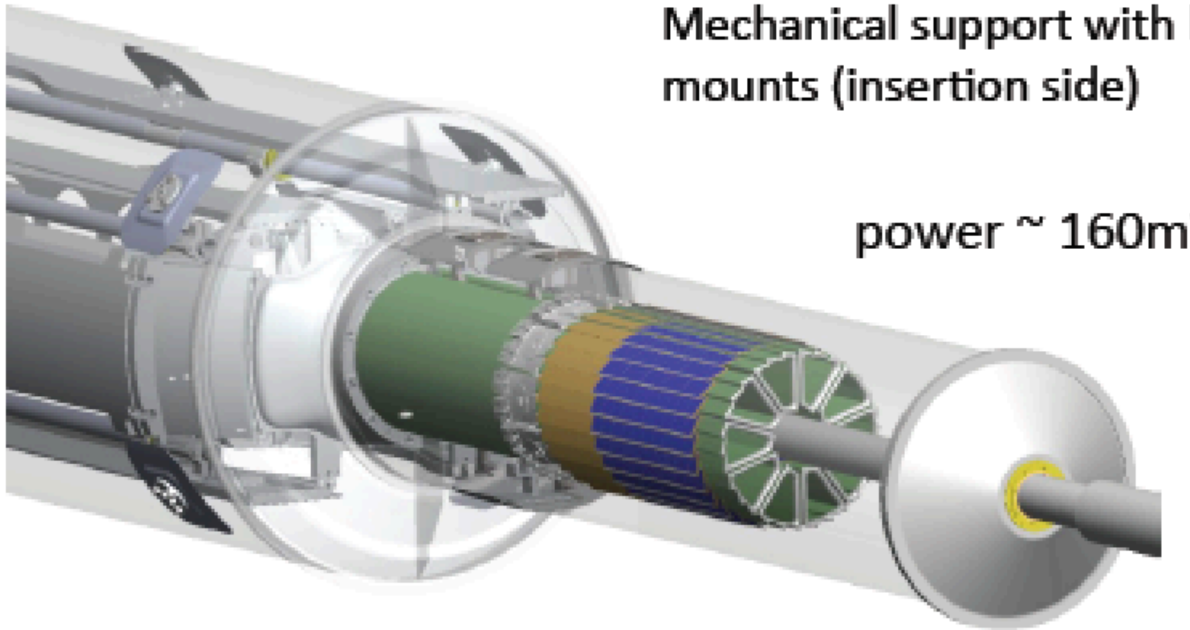
ALICE ITS Upgrade (and MFT)
$10\ \text{m}^2$ – 12 G pixel



sPHENIX
$0.2\ \text{m}^2$ – 251 M pixel

MAPS Application

STAR HFT - 1st application of MAPS



Mechanical support with kinematic mounts (insertion side)

power ~ 160mW/cm²

- 2 layers
- 10 sectors total (in 2 halves)
- 4 ladders/sector

Rolling Shutter
~180μs integr. time

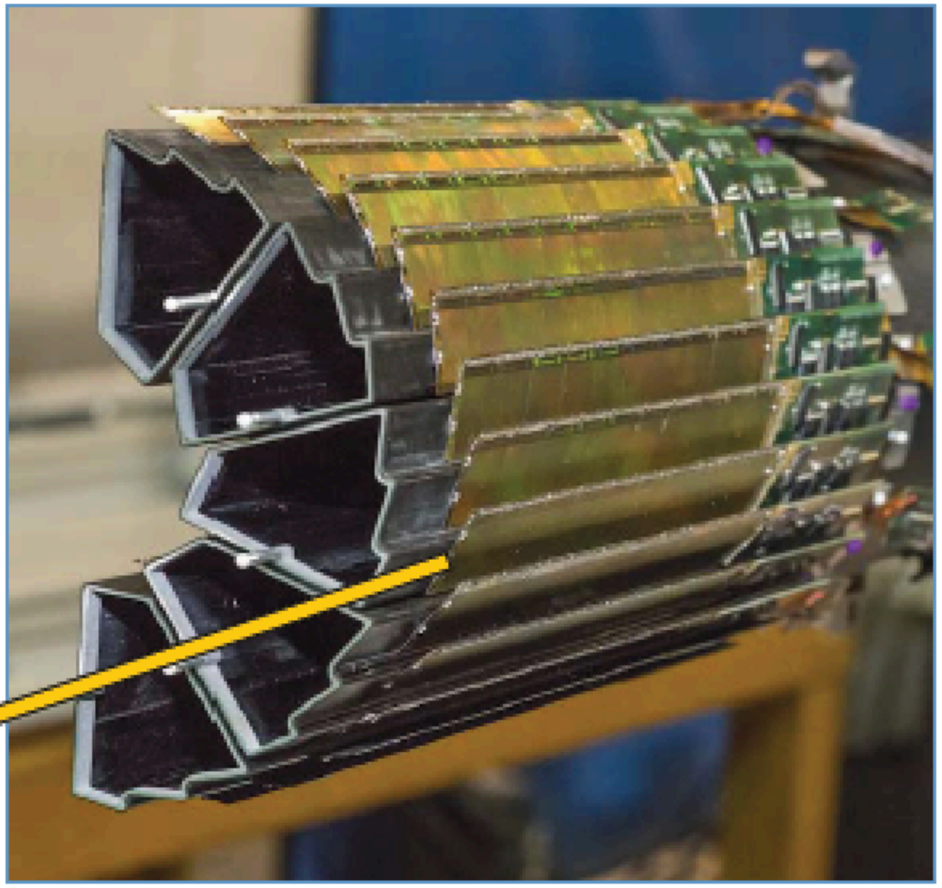
Ladder with 10 MAPS sensors (~ 2×2 cm² each)

2-layer kapton flex cable with Al traces

← 20 cm →

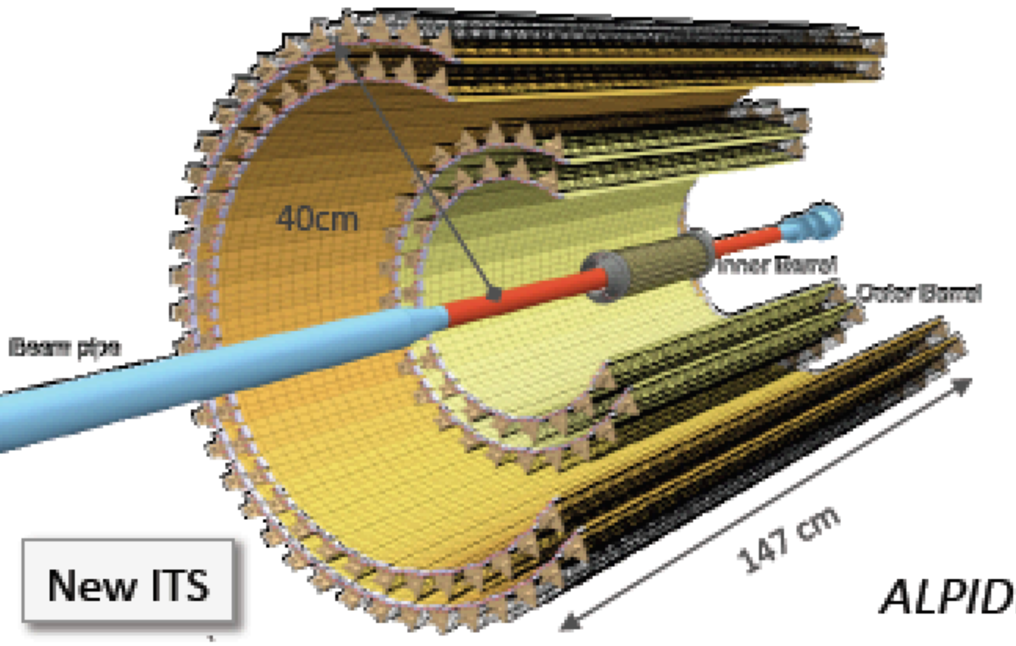
Key dates

- 3-sector prototype May 2013
- **Full detector Jan 2014**



carbon fiber sector tubes
(~ 200 μm thick)

ALICE New ITS - Closer, Thinner, Smaller



$-1.5 \le \eta \le 1.5$

Closer to IP: 39mm ➡ 22mm

Thinner: ~1.14% ➡ ~ 0.3% (for inner layers)

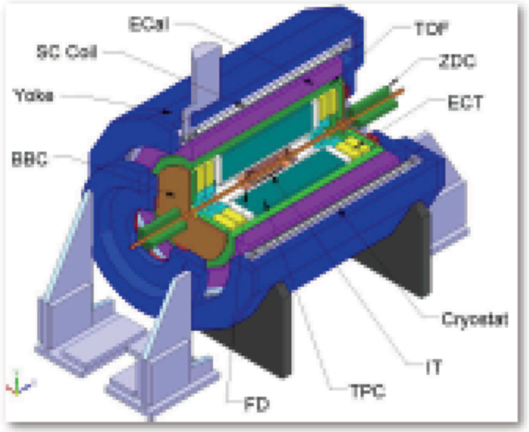
Smaller pixels: 50µm x 425µm ➡ 27µm x 29µm

Increase granularity (x 10^3): 20 chan/cm^3 ➡ 2k pixel/cm^3

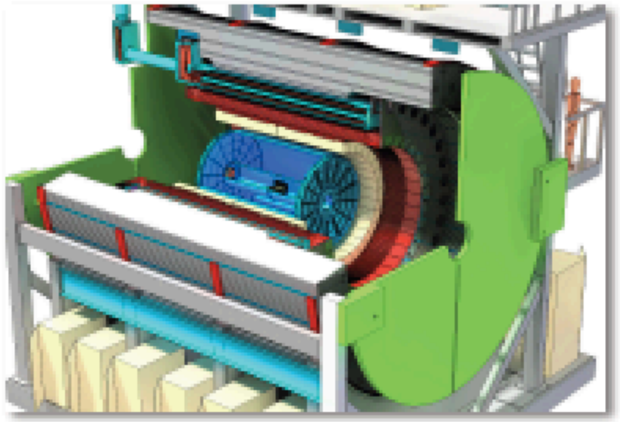
10 m^2 active silicon area: 12.5 G-pixels, $\sigma \approx 5\mu m$

*ALPIDE (**AL**ICE **Pi**xel **De**tector) - Developed for the ALICE upgrade (ITS and MFT) will be used (or it is proposed) for several other HEP detectors and non HEP applications*

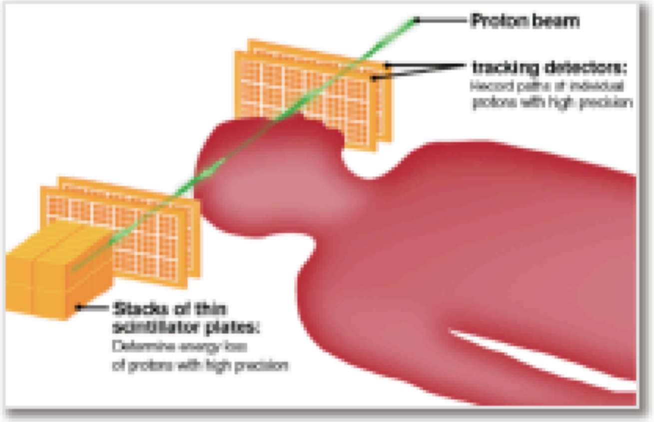
NICA MPD (@JINR)



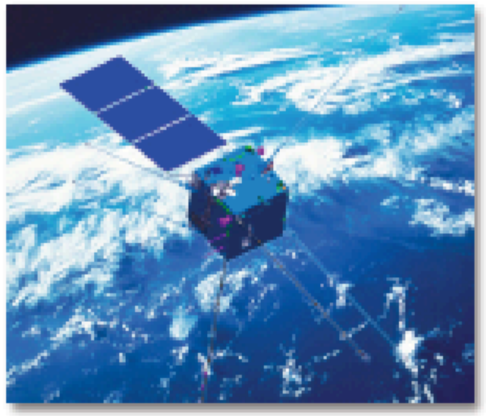
sPHENIX (BNL)



proton CT (tracking)



CSES – HEPD2



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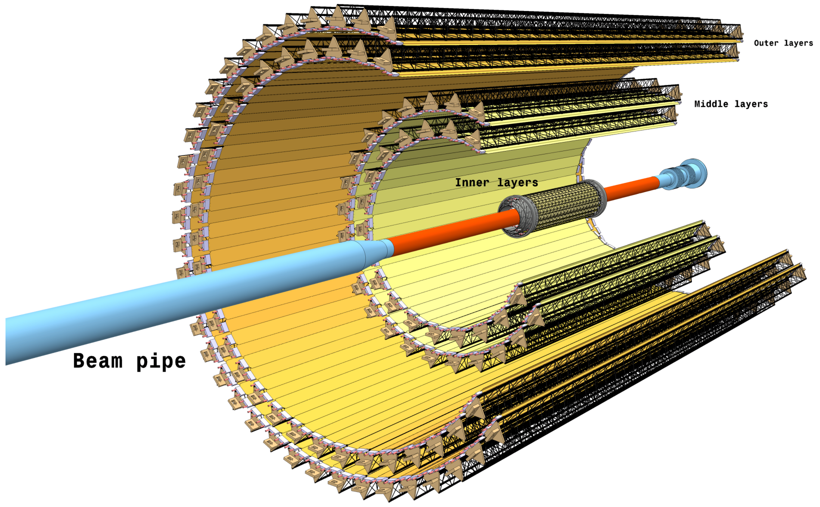
ALICE ITS Upgrade Ongoing

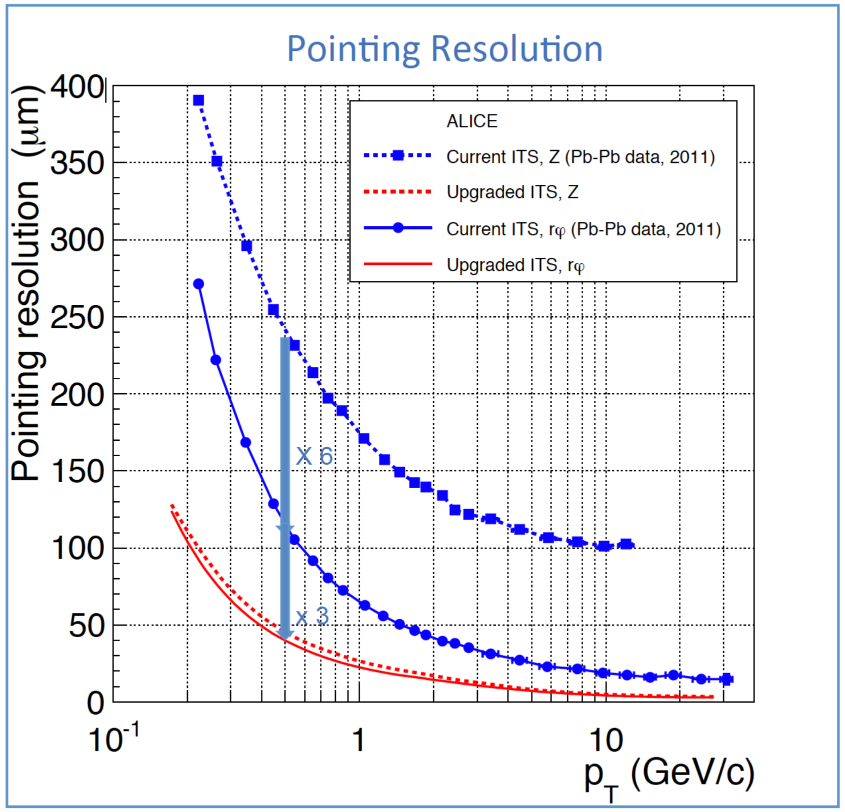
- Main detector requirements
  - Higher tracking efficiency and resolution at low p_T
    - Granularity ⬆ Material budget ⬇
  - High-statistics, un-triggered data sample
    - RO rate ⬆ Data size ⬇ (Online)



➡ New Silicon Tracker (**I**nner **T**racking **S**ystem) for HL LHC (installation during 19/20)

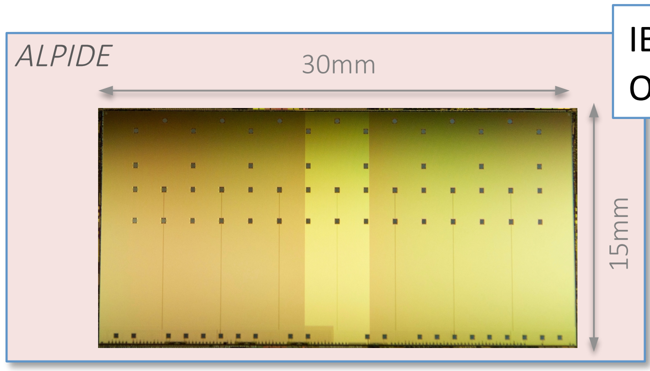
- Improve impact parameter resolution by a factor of 3
  - Get closer to IP (1st layer): 39 - 430mm ➤ 23 - 400mm ($|\eta| \leq 1.22$)
  - Material budget X/X0 per layer: ~1.14% ➤ ~0.3% (inner)
  - Reduce pixel size: 50μm x 425μm ➤ 28μm x 28μm
- Improve tracking efficiency and p_T resolution at low p_T
  - Increase granularity: 6 layers ➤ 7 layers w. reduced pixel size
- Fast readout: 1 kHz (1kHz) in PbPb (pp) ➤ 100 kHz (400kHz) in PbPb (pp)
- Power density < 40mW/cm^2
- Fast insertion/removal for yearly maintenance

Impact parameter resolution



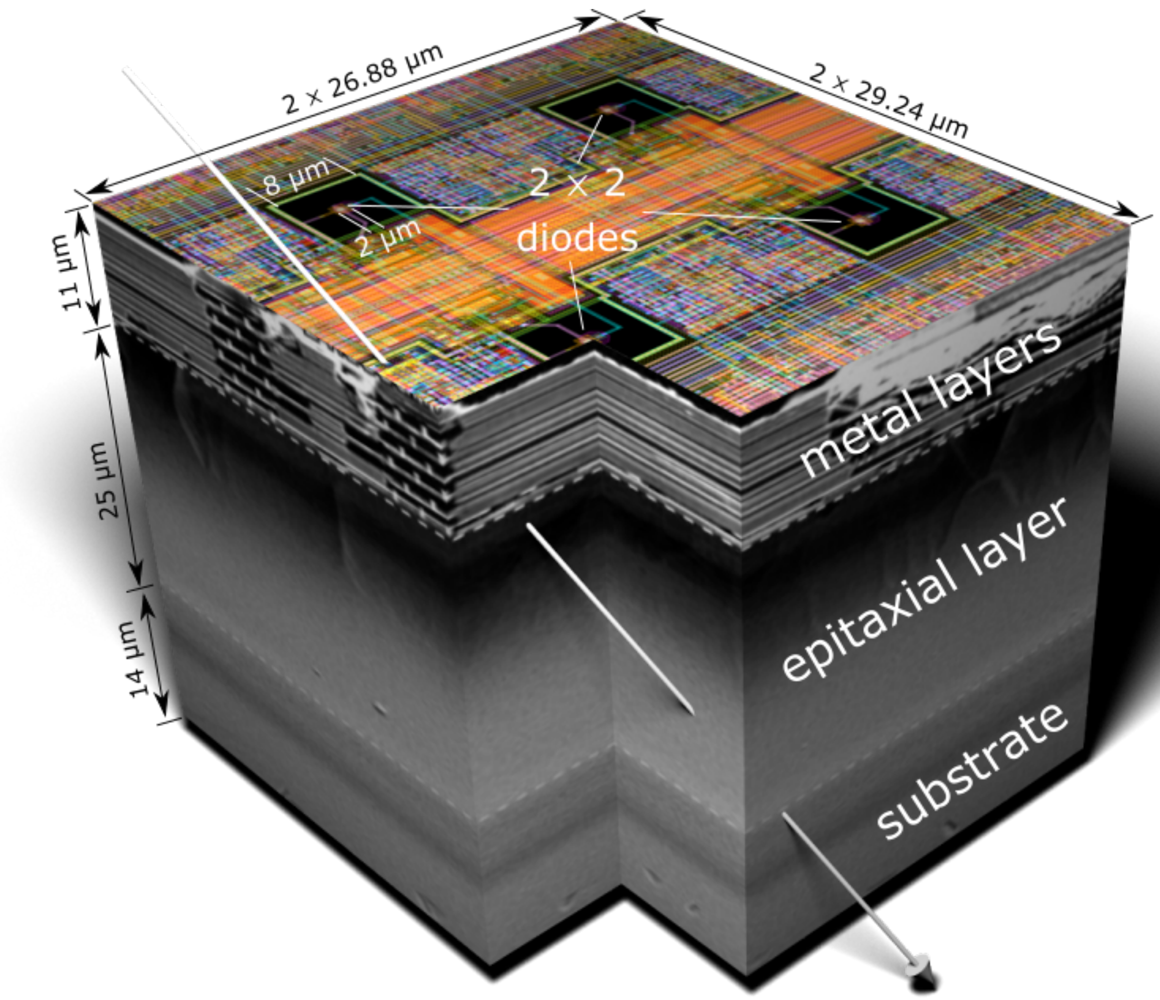
ALPIDE (ALice PIxel DEtector)

- CMOS Pixel Sensor using 0.18μm CMOS Imaging Process
  - High-resistivity (>1kΩ·cm) p-type epitaxial layer (25μm) on p-type substrate
  - Small n-well diode (2μm ϕ) ~ low capacitance (fF)
  - $-6V < V_{BB} < 0V$ to increase depletion zone around n-well diode
  - Deep p-well shields n-well of PMOS transistors
- Full CMOS circuitry within active area



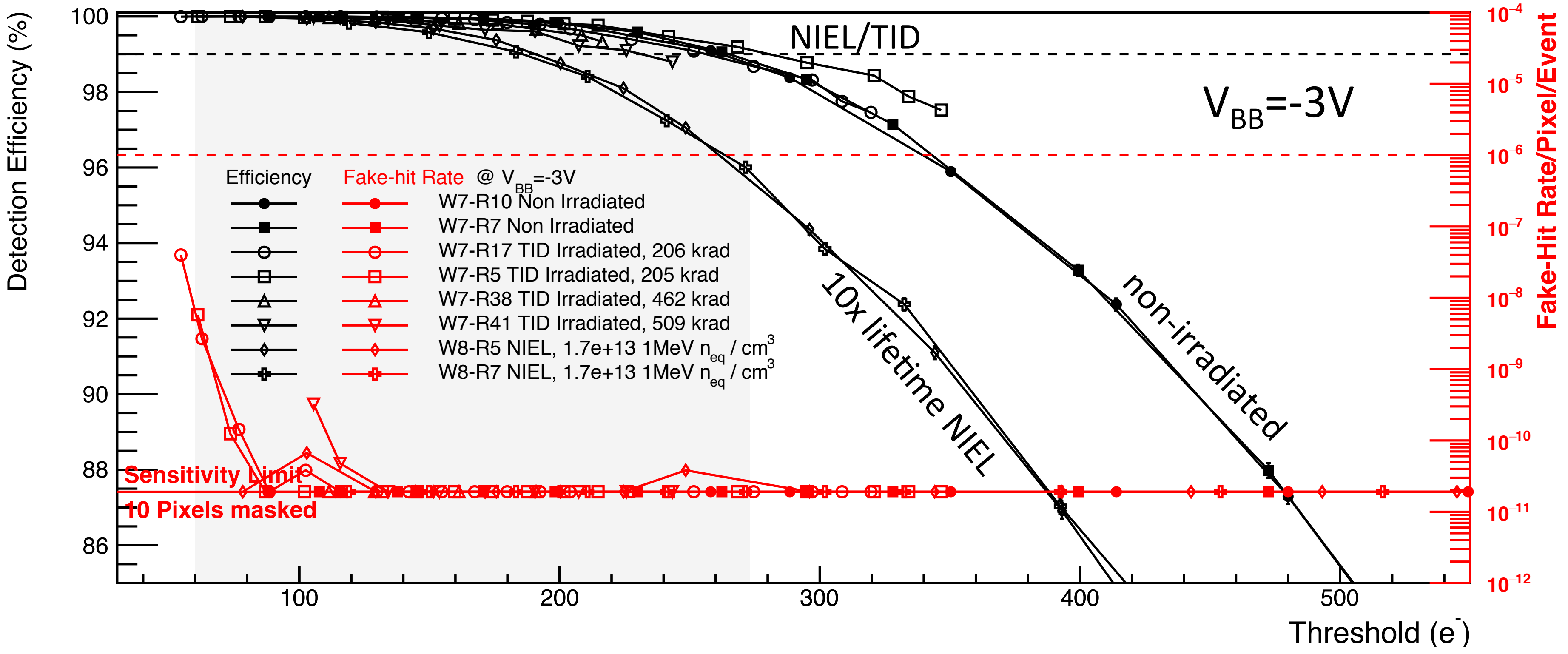
IB: 50μm thick
OB: 100μm thick

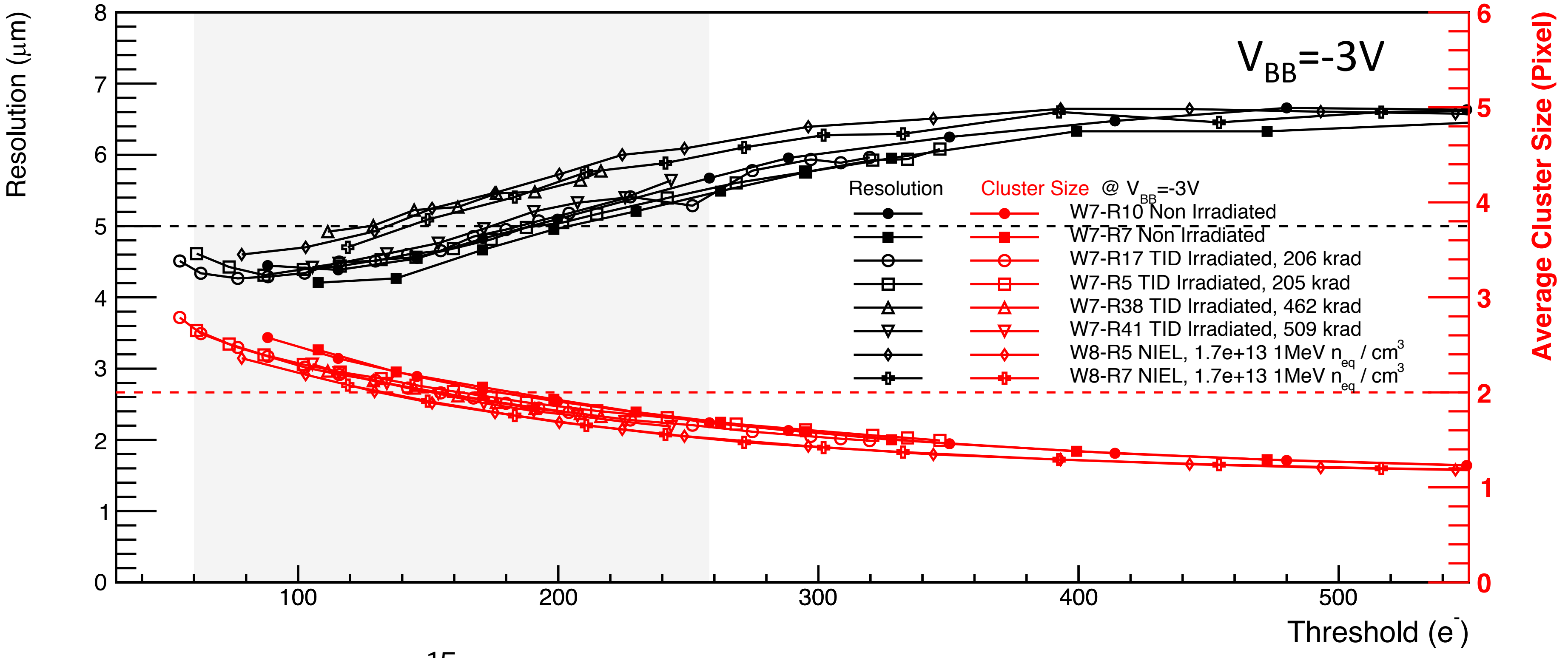
- Pixel: $27 \times 29 \times 25\ \mu m^3$
- 130,000 pixels/cm^2 ~ Total $10 m^2$, 12.5 G-pixels
- Spatial resolution ~ 5μm in 3D
- Max. particle rate: 100MHz/cm^2
- fake-hit rate ~ 10^{-10} pixel/event
- Power ~ 300 nW/pixel



ALPIDE (ALice PIxel DEtector) Performance

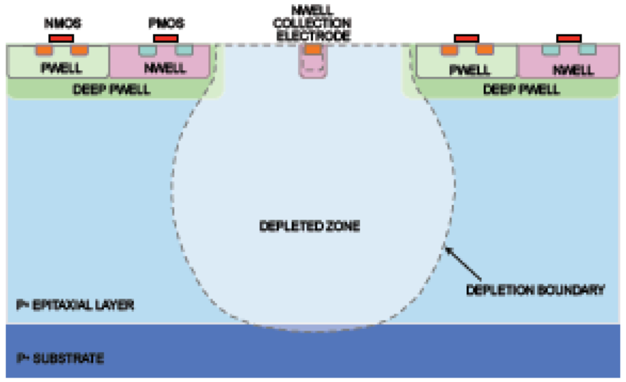
- Detection efficiency and Fake-hit rate
- Resolution and Cluster size
  - Non-irradiated and NIEL/TID chips ~ similar
  - Sufficient operational margin after 10 x lifetime NIEL dose
  - Resolution < 5μm at Threshold < 150 e
  - Resolution ~ 6μm at Threshold of 300 e
  - Chip-to-chip fluctuations negligible



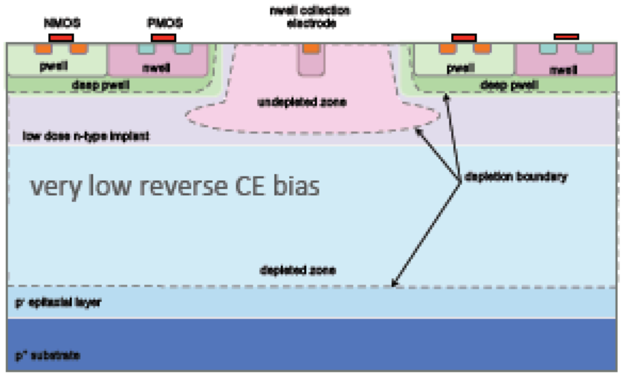


MAPS fully depleted

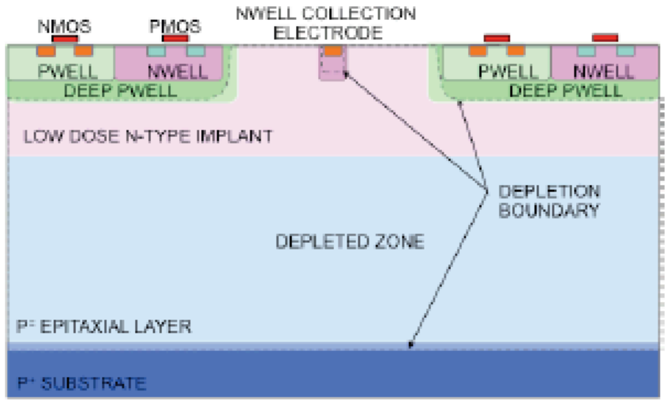
Fully depleted MAPS



Standard Process (+DEEP PWELL)

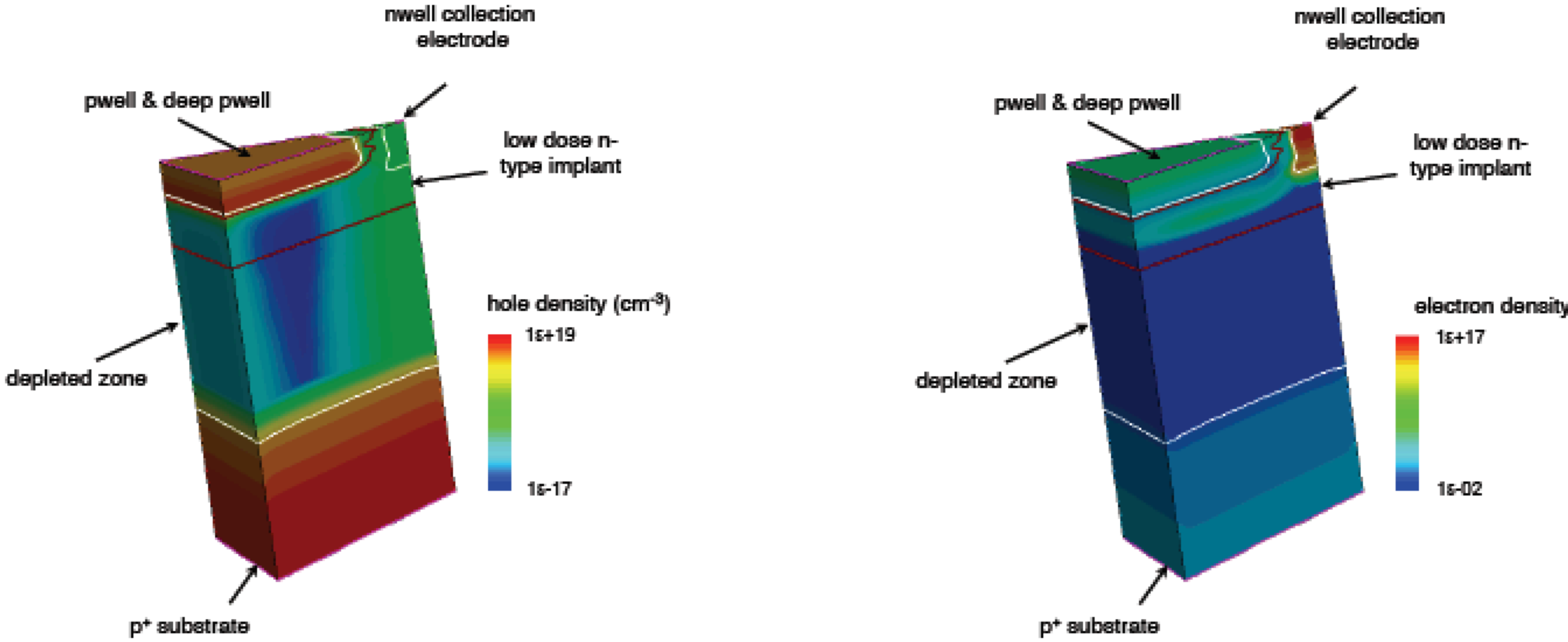


Modified Process with low-dose n-type implant (+DEEP P



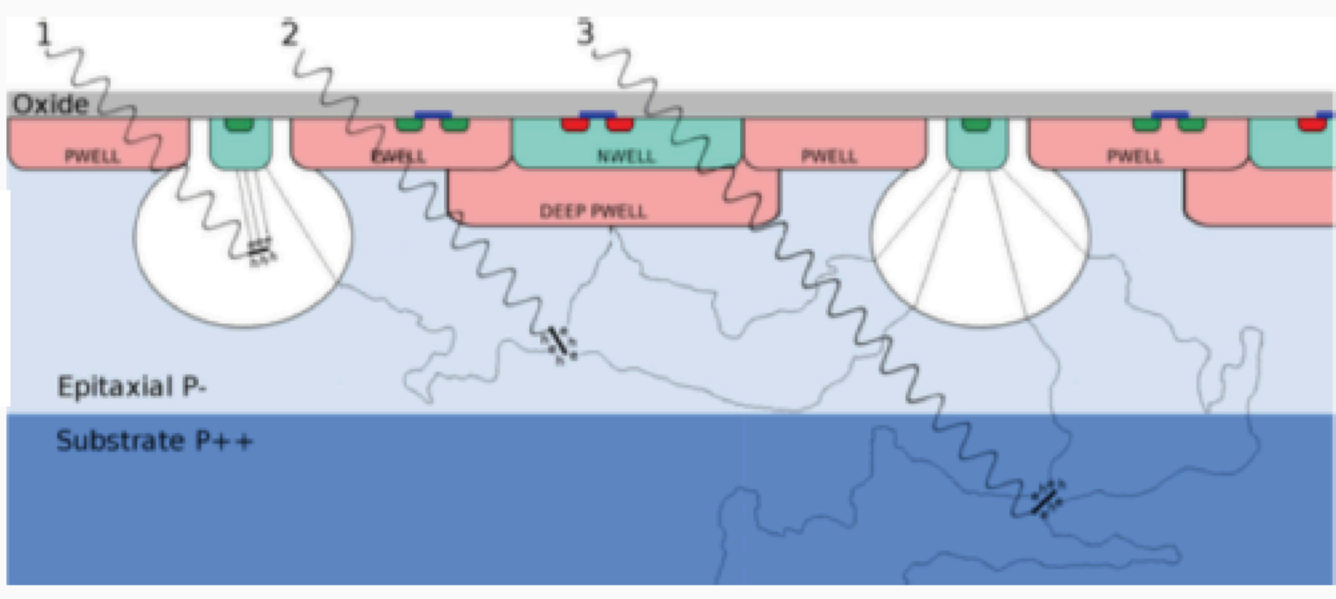
higher reverse CE bias

- Process modification for enhanced depletion, timing performance and radiation tolerance
- NIM A 871C (2017) 90-96 (CERN/Tower)
- ALICE R&D chip: INVESTIGATOR
- Moderation of Vbb ~ -5V



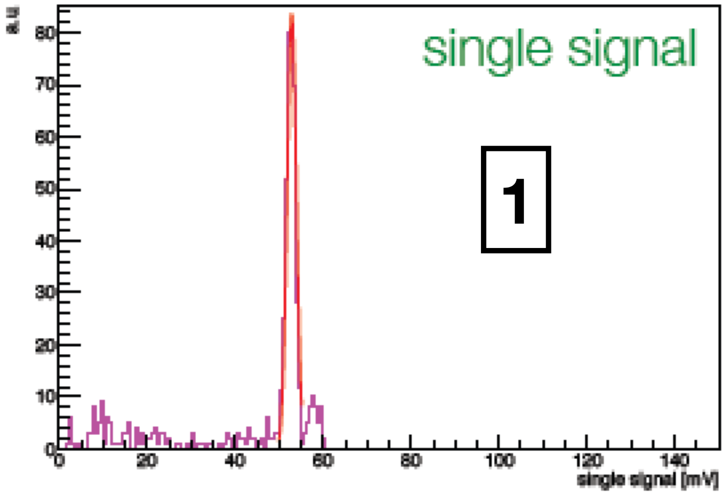
High-res = 18μm, V_{CE} = 5V, $V_{substrate}$ = -15V

A Process modification for full depletion



^{55}Fe: two X-Ray emission modes:

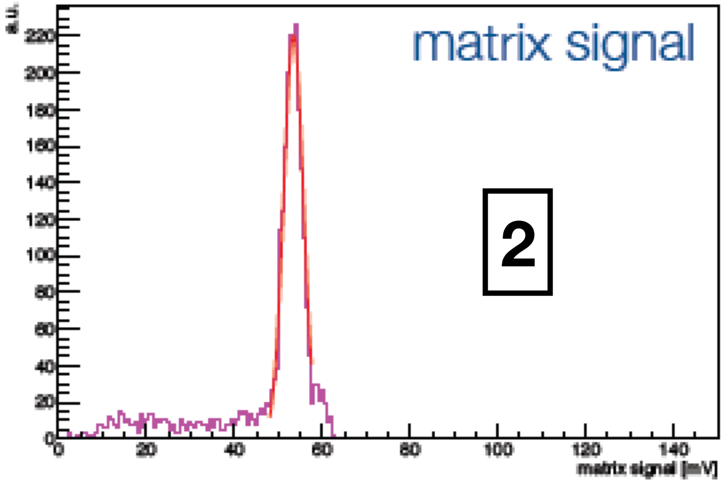
1. K-α: 5.9 keV (1640 e/h), rel. freq.: 89.5% atten. length in Si: 29μm
2. K-β: 6.5 keV (1800 e/h), rel. freq.: 10.5% atten. length in Si: 37μm



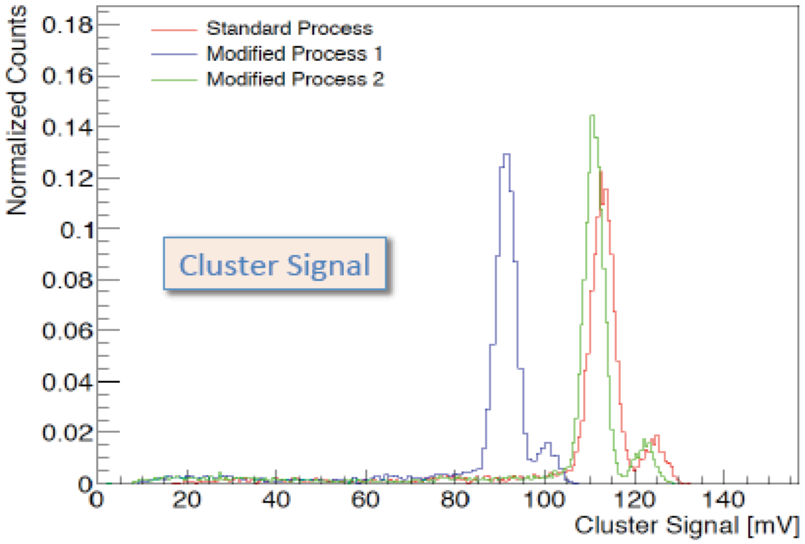
1. Absorption in depletion region: Charge collection by drift (~1ns); no charge sharing; single pixel cluster (:= calibration peak)

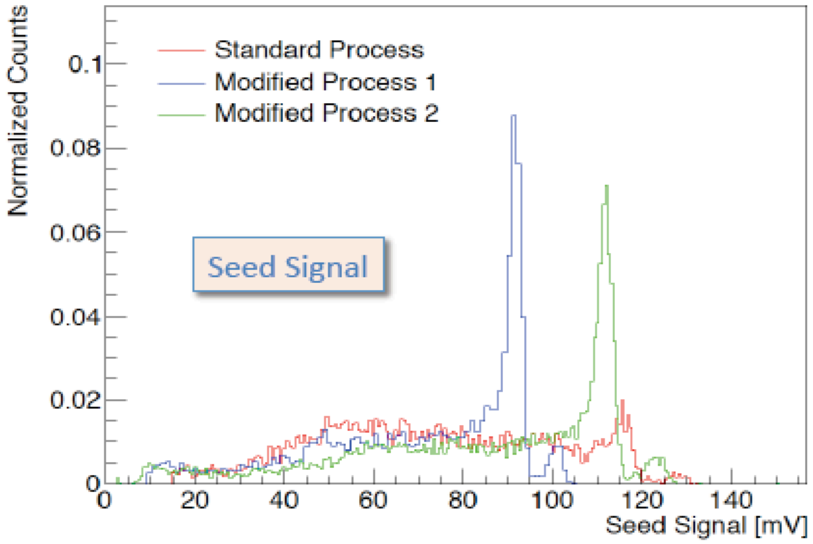
2. Absorption in epitaxial layer: Charge collection partially by diffusion + drift; charge sharing depending on distances

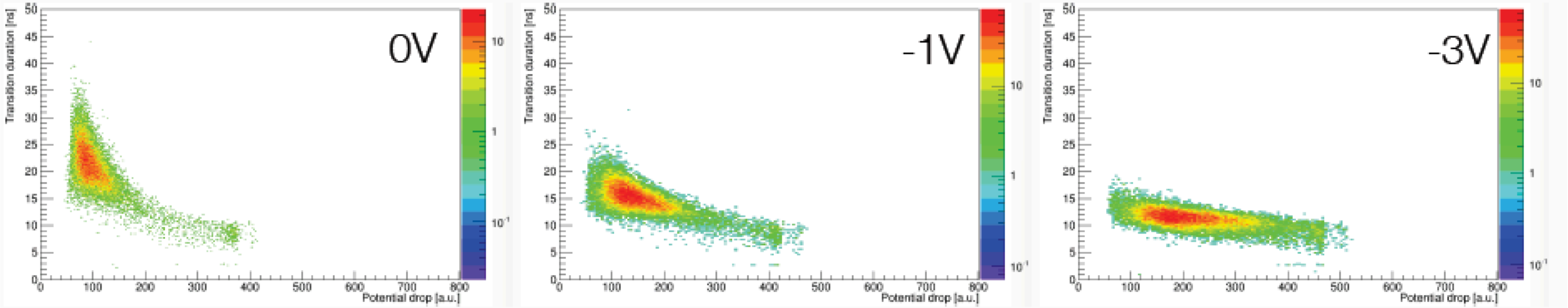
3. Absorption in substrate: Charge collection depending on depth and lifetime of charge carrier



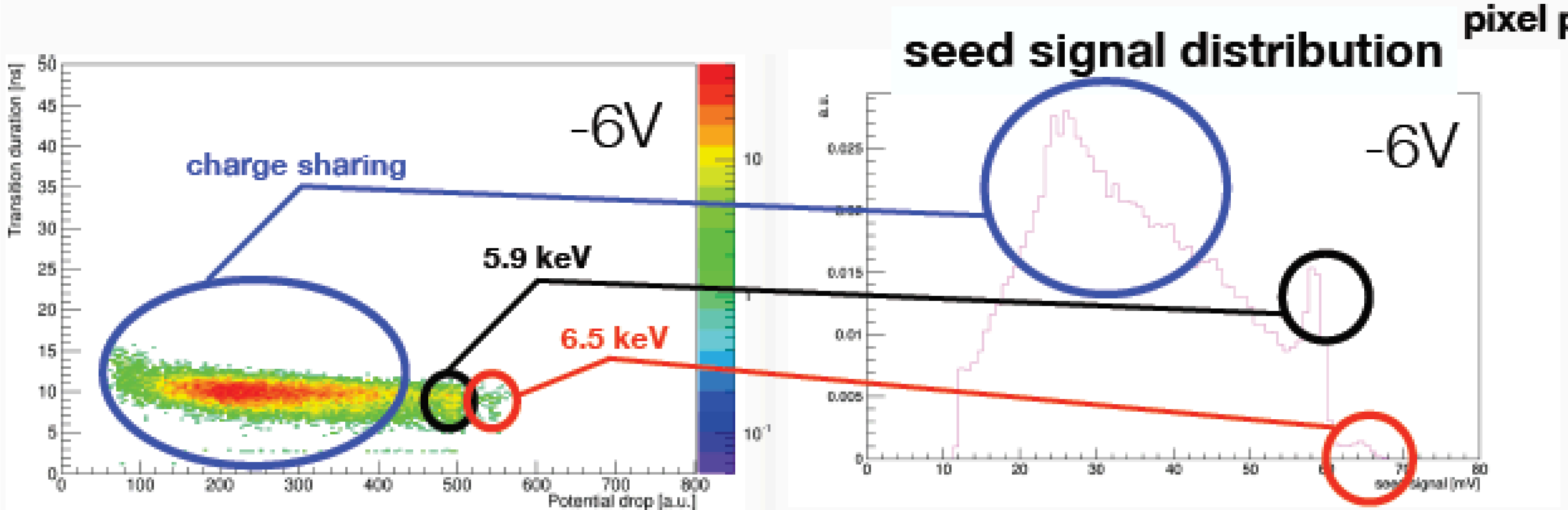
modification R&D ongoing







pixel pitch: 20 μm, N-well size: 3 μm, spacing: 1 μm

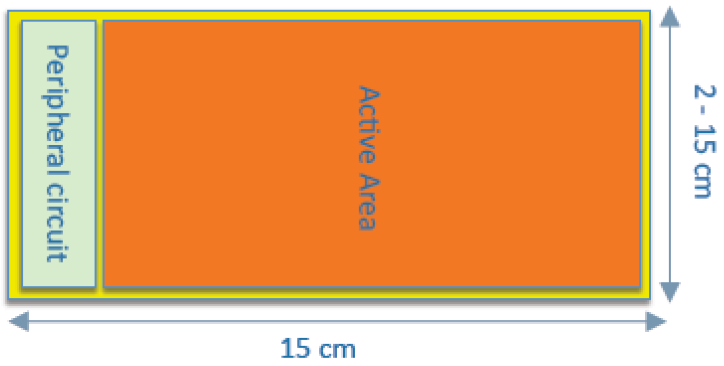


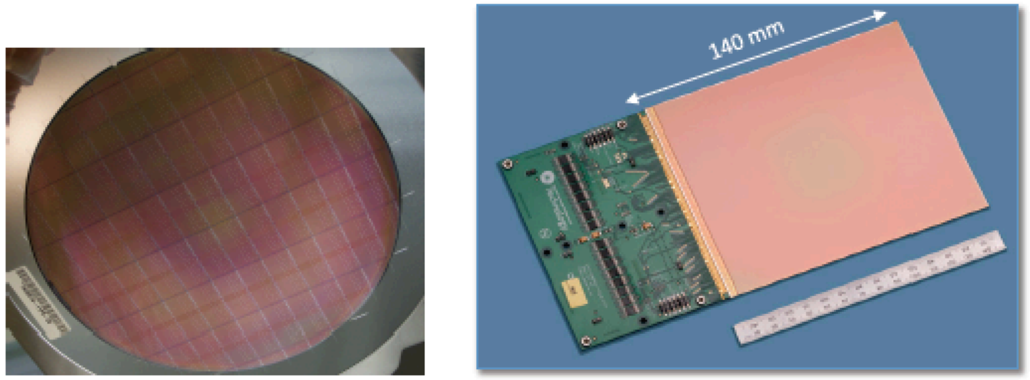
acknowledge to SHLee

Innovative Ideas & Technology

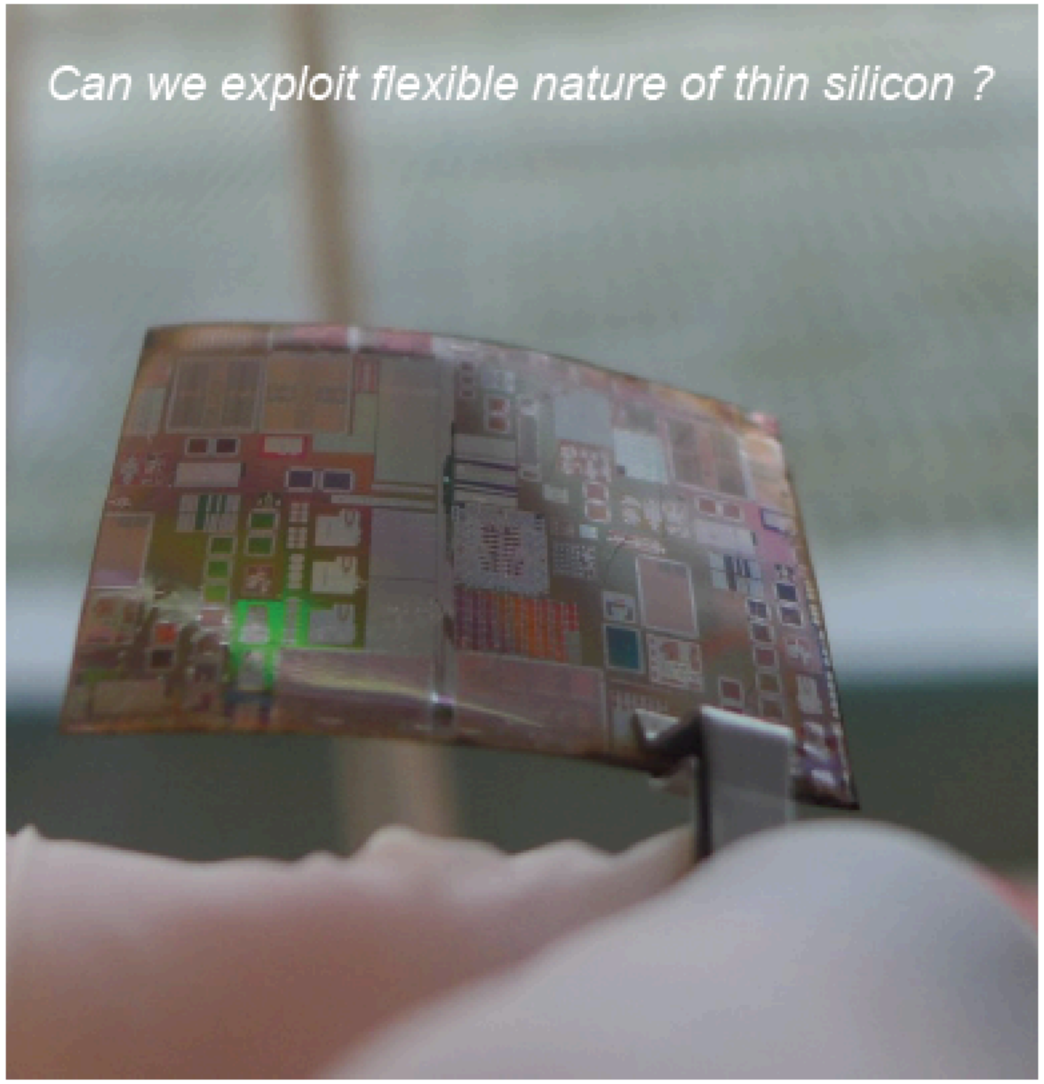
Technology and Innovation

1-D or 2-D stitched version of a sensor chip





Stitching available also for 300mm technologies



Can we exploit flexible nature of thin silicon ?

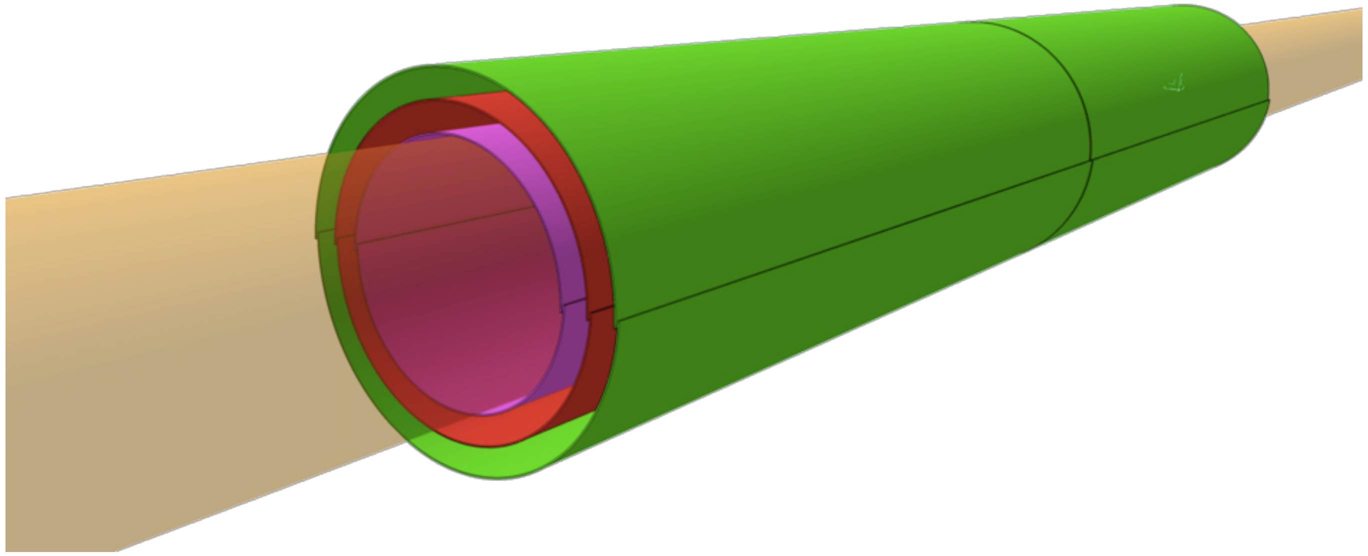
Chipworks: 30µm-thick RF-SOI CMOS

Ultra-thin chip (<50 um): flexible with good stability

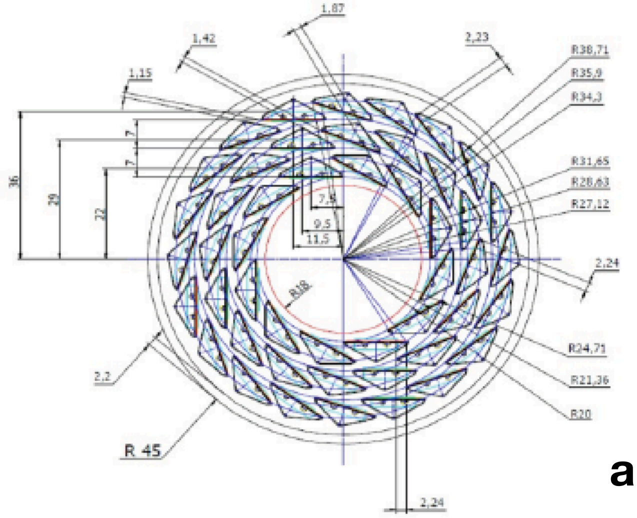
Silicon Genesis: 20 micron thick Si wafer

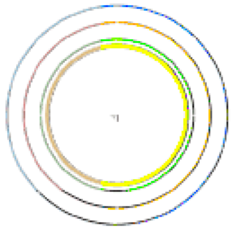
IDEAL Vertex Tracker (only with Si)

- Detection efficiency ➔ 100%
- Material budget (X/X0) ➔ 0%
- Power consumption ➔ 0 ➔ no cooling



Comparison with present IB

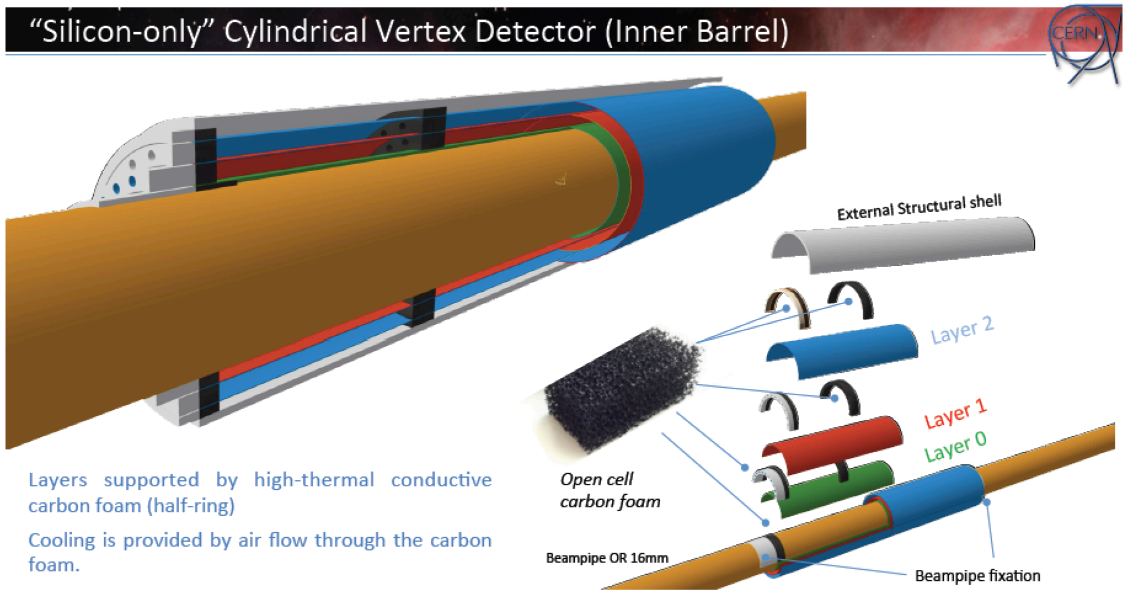




acknowledge to Dainese

	Radius	x/X0
Pipe	19mm	0.22%
L0	23mm	0.3%
L1	31mm	0.3%
L2	39mm	0.3%

	Radius	x/X0
Pipe	16mm	0.22%
L0	18mm	0.05%
L1	24mm	0.05%
L2	30mm	0.05%



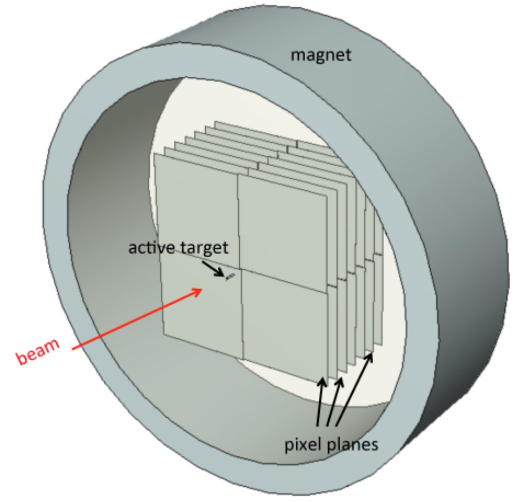
“Silicon-only” Cylindrical Vertex Detector (Inner Barrel)

Layers supported by high-thermal conductive carbon foam (half-ring)

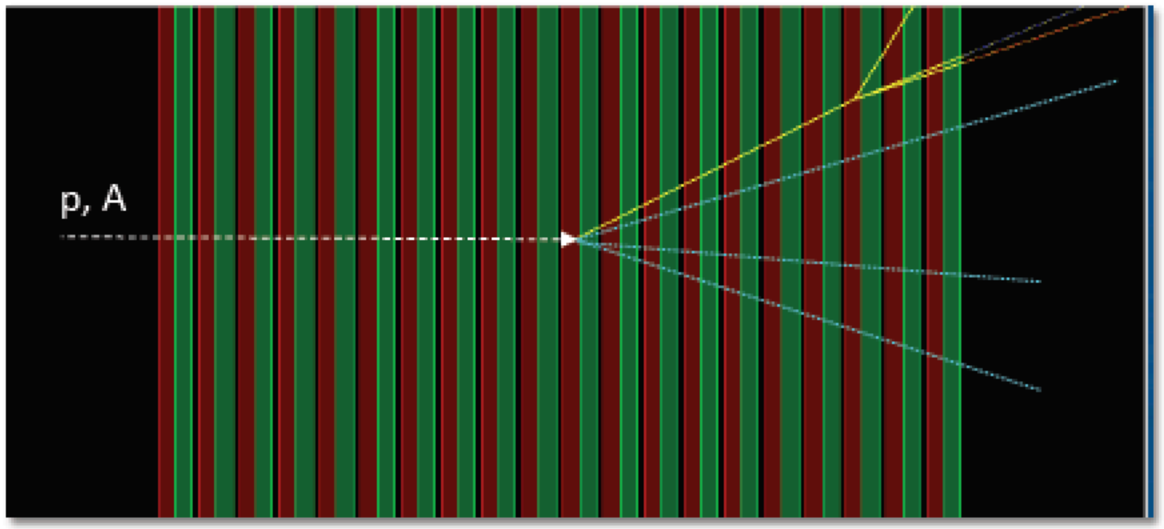
Cooling is provided by air flow through the carbon foam.

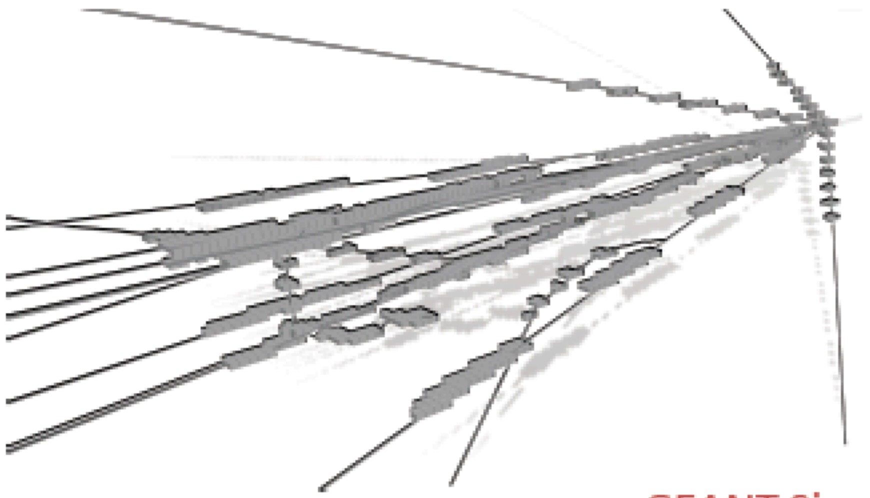
Furthermore …

- Even “Starting detection at IP” with ‘active’ target



A different configuration based on planes transverse to the beam direction



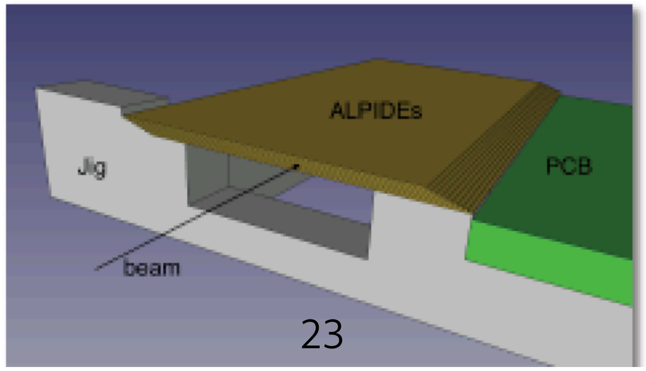


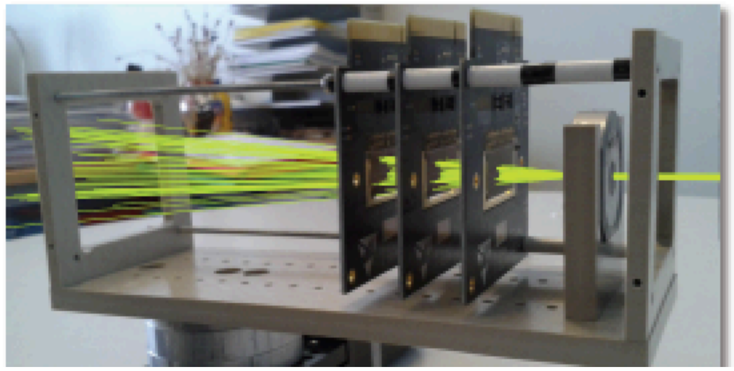
GEANT Simulation

The target is a different material, which is used as support and cold plate for the sensors

Demonstrator will be tested at SPS summer 2018

Pixel Chamber + telescope to measure beam position and emerging particles





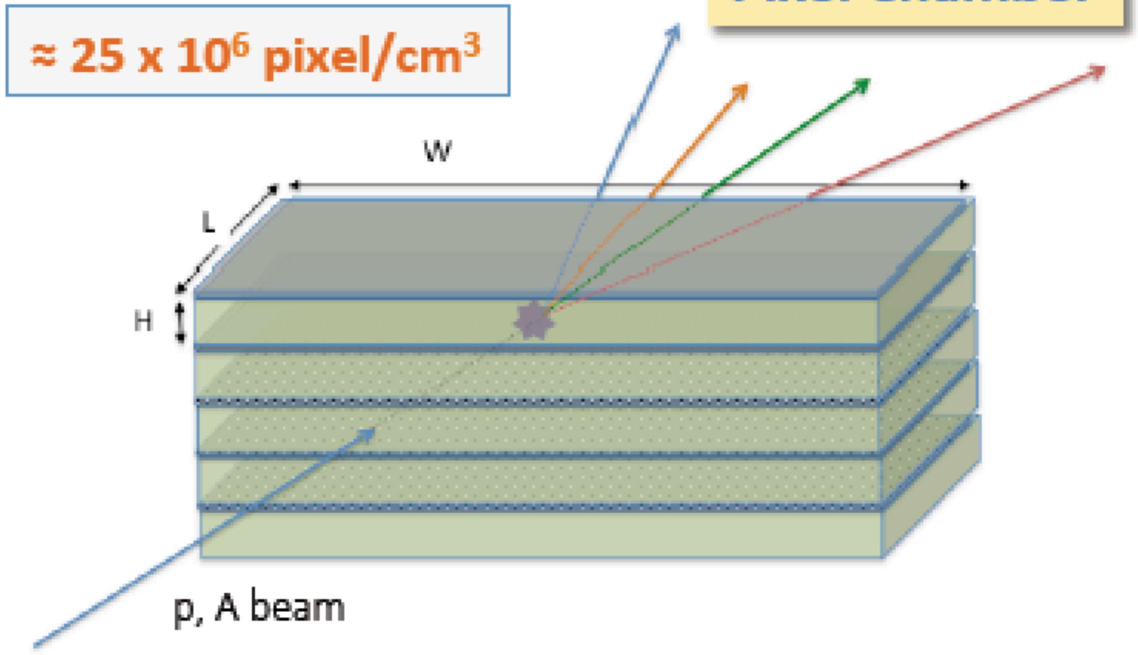
even 3D Silicon Pixel chamber

Studies on 3D Pixel Chamber Imager for measuring charm and beauty at a fixed target experiment

The heart is a **3D pixel chamber** used as active target

The idea is to have a detector able to provide the image of the proton-nucleus or nucleus-nucleus interaction and track the particles generated in the inelastic collision just starting at the interaction point

The pixel chamber is realized with a stack-up of thin CMOS sensors providing truly 3D (almost) continuous tracking with a precision of few microns for very high rate and multiplicity environment



≈ 25 x 10^6 pixel/cm^3

Pixel Chamber

Nuclear interaction inside a stack-up of N fine pitch pixel sensor

- N ≈ 100 , H ~ 50µm, L ≈ 0.1 nuclear collision length (≈30mm)
- *cm boost: ≈ 14 at 400 GeV/c (SPS), ≈60 at 7TeV (LHC)*

ALICE (only with) S(ilicon)

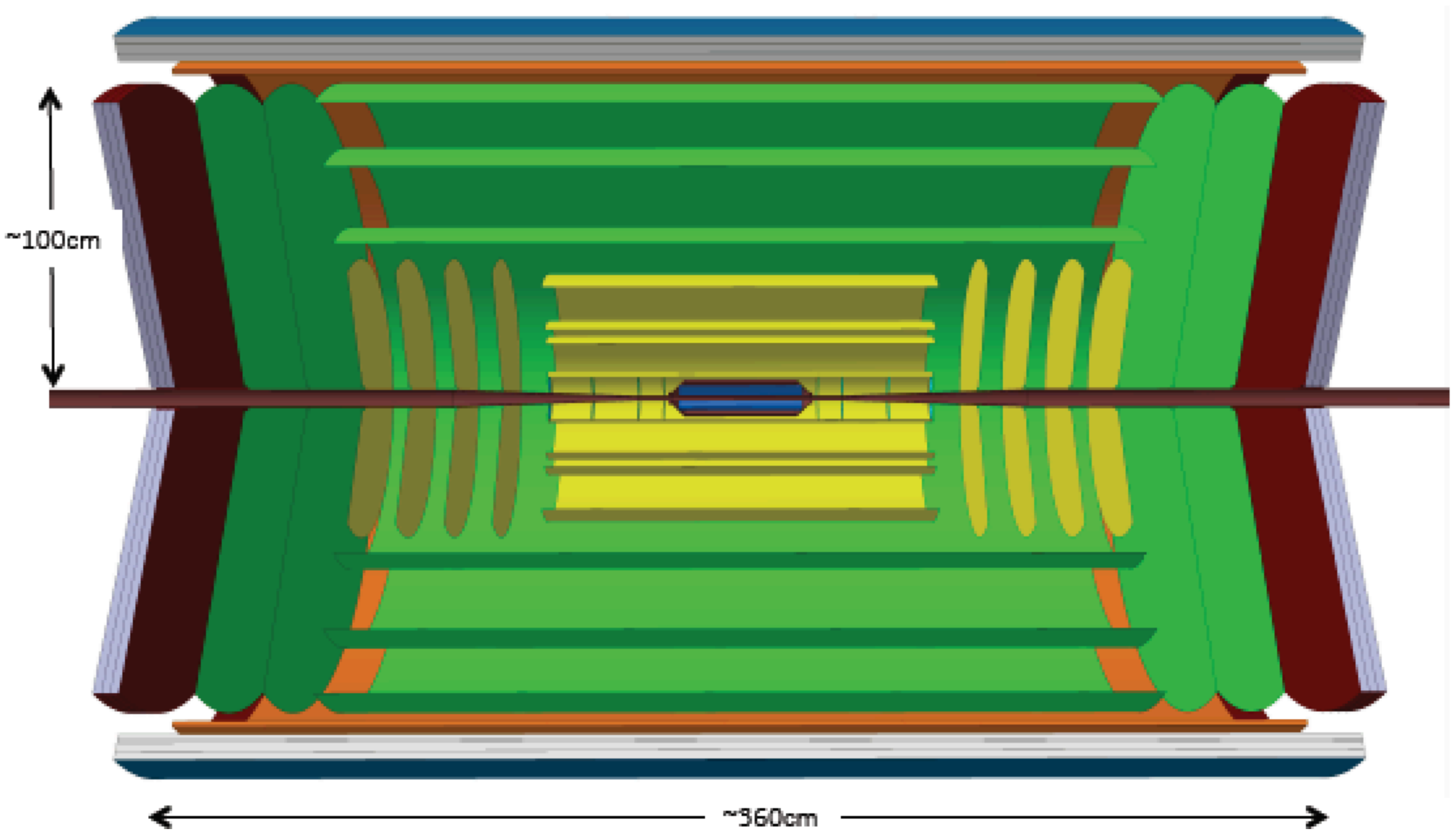
A new experiment based on a “all-silicon” detector

Tracker: ~10 tracking barrel layers (blue, yellow and green) based on CMOS sensors

Hadron ID: TOF with outer silicon layers (orange)

Electron ID: pre-shower (outermost blue layer)

Extended rapidity coverage: **up to 8 rapidity units**
+ FoCal



Preliminary studies

Magnetic Field
- B = 0.5 or 1 T

Spatial resolution
- Innermost 3 layers: $\sigma \sim 1\mu m$
- Outer layers: $\sigma \sim 5\mu m$

Time Measurement
Outermost layer integrates high precision time measurement ($\sigma_t < 30ps$)

ALICE proposal for LS4 (2030) officially submitted by PBM, LM and F. Antinori for ALICE collaboration (Dec. 2018)

A Lesson from Technology

KoALICE

> Scientific Advance is more often driven by the development of a <u>NEW tool</u> than a new concept
>
> - Freemab Dyson