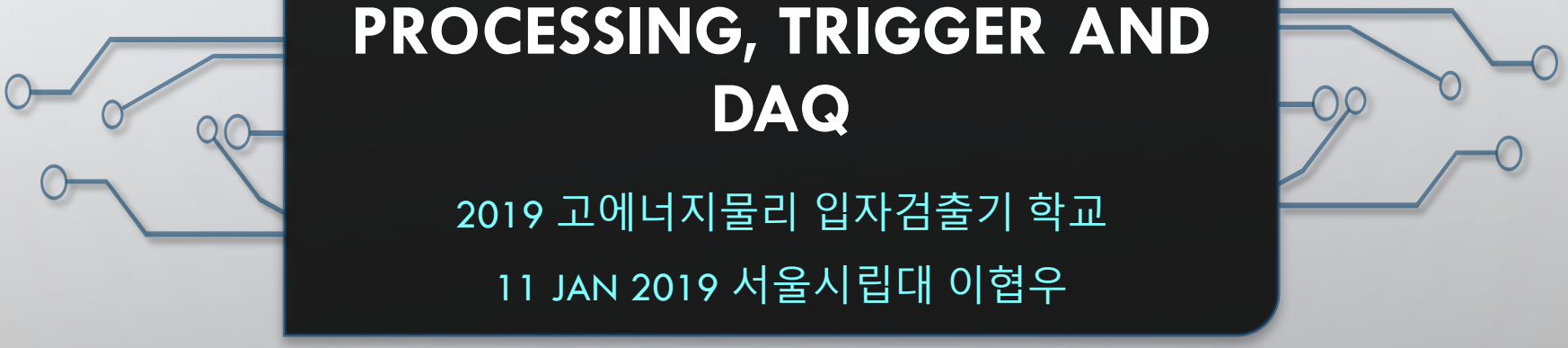


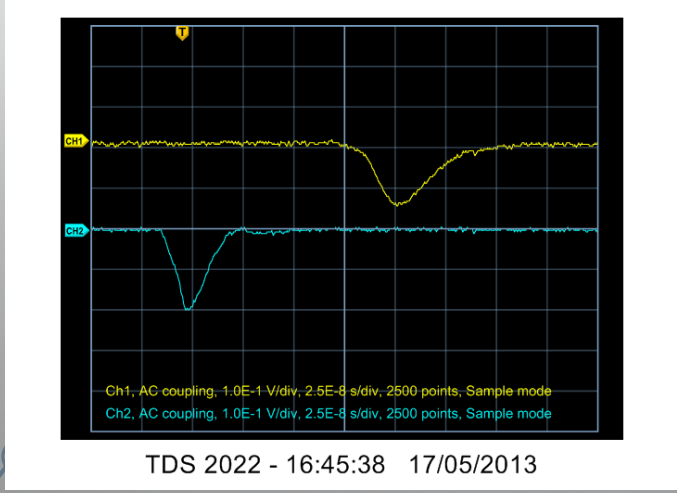
BASICS OF SIGNAL PROCESSING, TRIGGER AND DAQ

2019 고에너지물리 입자검출기 학교

11 JAN 2019 서울시립대 이협우

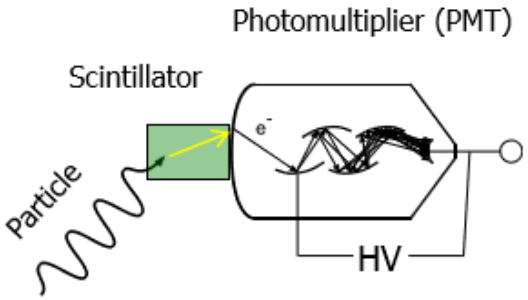
CAVEAT

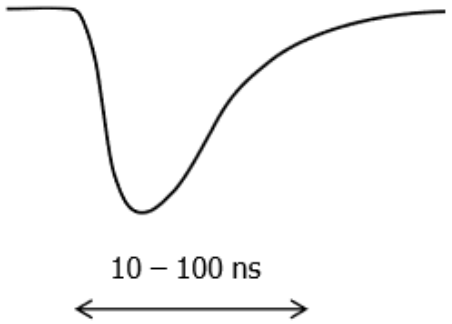
- ISOTDAQ(International School of Trigger and Data Acquisition)
- Signal Processing – Analog to digital
- Trigger and DAQ Hardware
- Simple Example - Energy measurement (Scintillator+PMT)



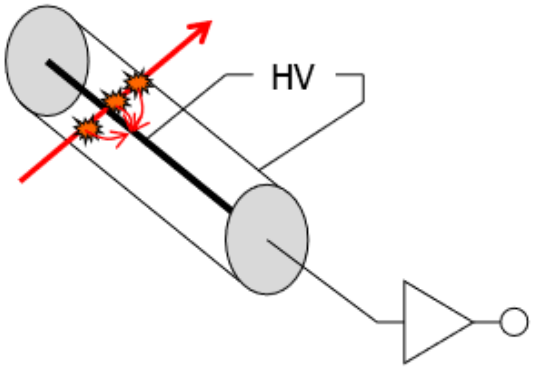
SIGNALS IN PARTICLE PHYSICS

Scintillators (Plastic, Crystals, Noble Liquids, …)

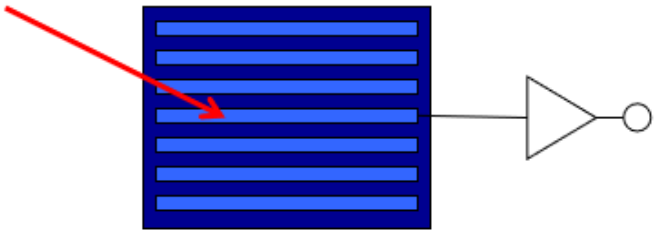


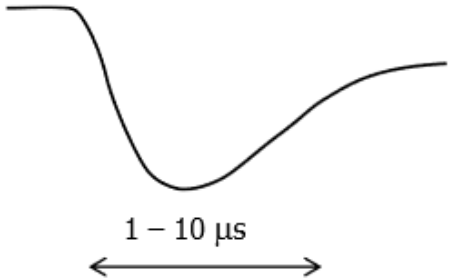


Wire chambers
Straw tubes

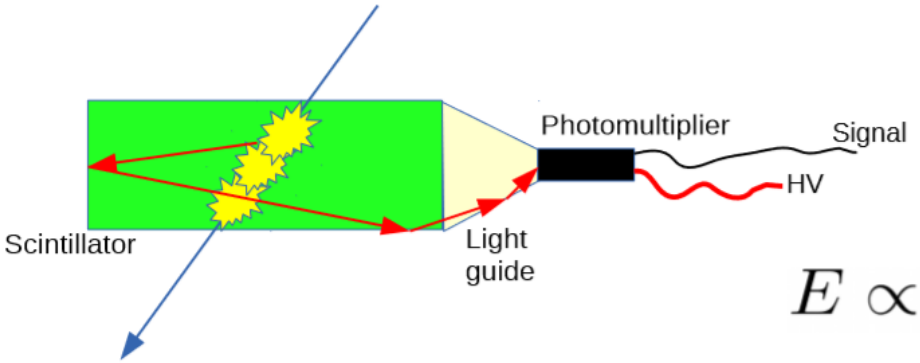


Silicon
Germanium

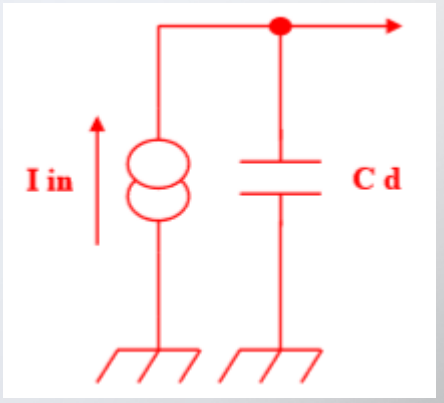


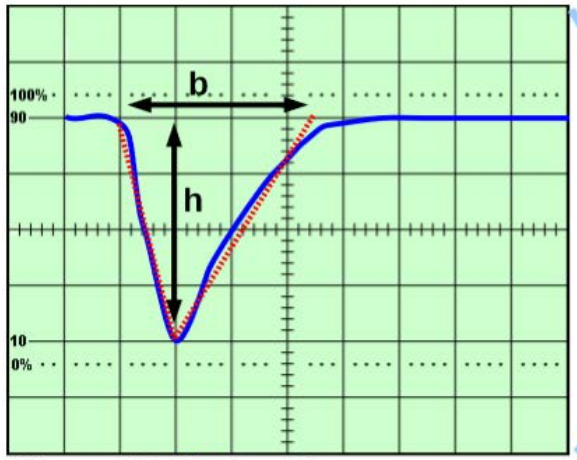


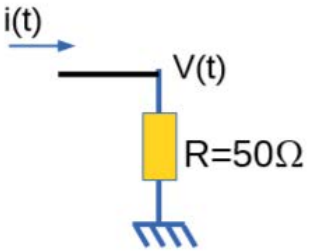
OSCILLOSCOPE



$$E \propto N_\gamma$$







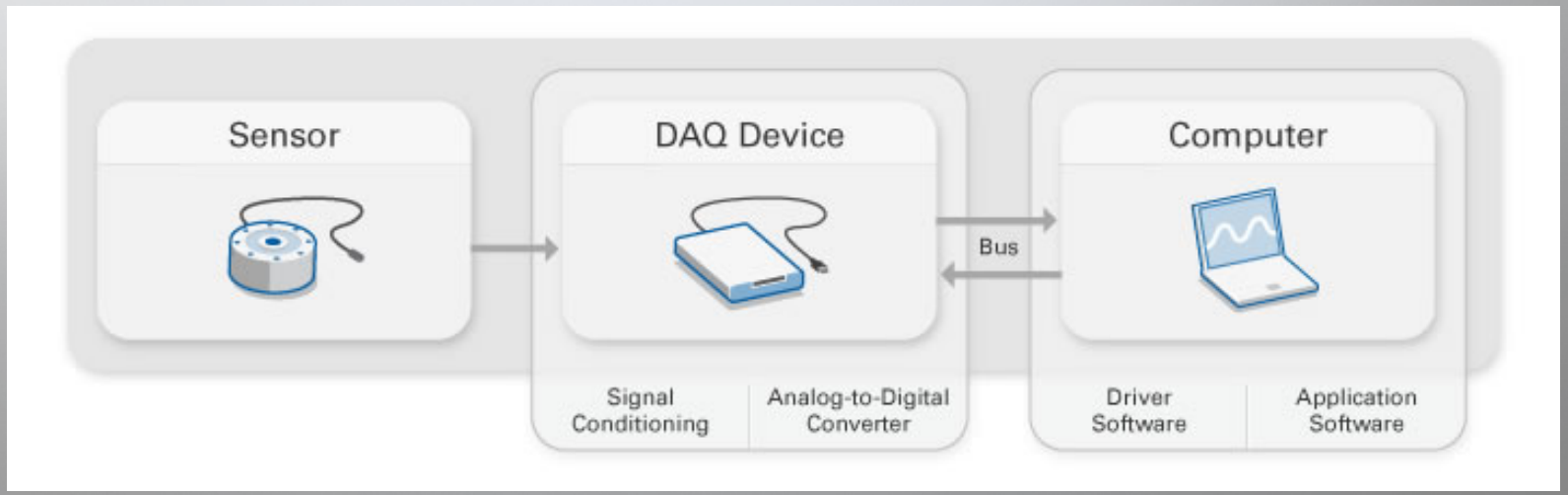
$$Q = \int i(t)\,dt = \frac{1}{R}\int V(t)\,dt$$

$$Q \approx \frac{1}{R}\frac{bh}{2} = \frac{1}{50\Omega}\frac{(3.5\cdot(20\text{ns}))(4\cdot(100\text{mV}))}{2} = 280\text{pC}$$

DAQ

Data acquisition (**DAQ**) is the process of measuring an electrical or physical phenomenon such as voltage, current, temperature, pressure, or sound with a computer. A **DAQ system** consists of sensors, **DAQ** measurement hardware, and a computer with programmable software.

What Is Data Acquisition? - National Instruments
www.ni.com/data-acquisition/what-is/



DAQ

- Gathers data produced by detectors: Readout
- Possibly feeds several trigger levels: HLT
- Forms complete events: Event Building
- Stores event data: Data Logging
- Provides Run Control, Configuration and Monitoring

TRIGGER

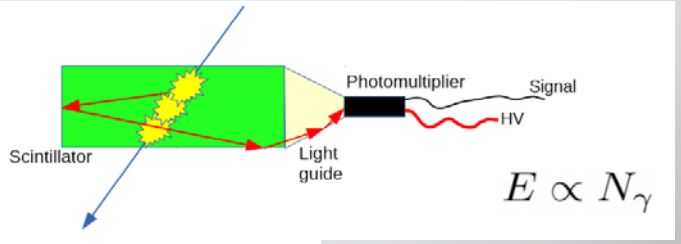
- Dictionary : to make a piece of equipment, etc. start working
- Wikipedia - Trigger (particle physics) : In particle physics, a trigger is a system that uses criteria to rapidly decide which events in a particle detector to keep when only a small fraction of the total can be recorded. Trigger systems are necessary due to real-world limitations in computing power, data storage capacity and rates. Since experiments are typically searching for "interesting" events (such as decays of rare particles) that occur at a relatively low rate, trigger systems are used to identify the events that should be recorded for later analysis…

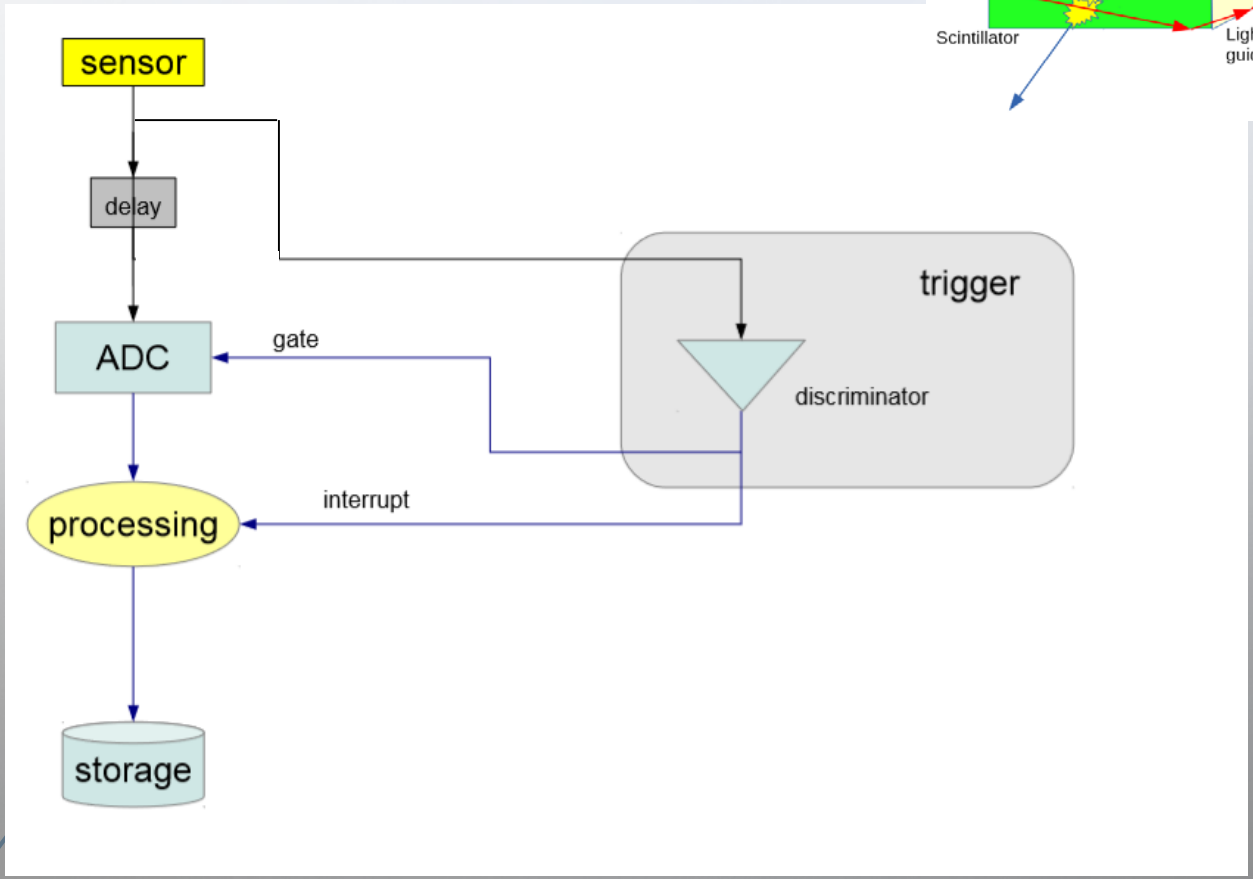
TRIGGER AND DAQ

- Self Trigger, External Trigger
- (Non-)Periodic Trigger
- Latency
- Dead time

SIMPLE EXAMPLE

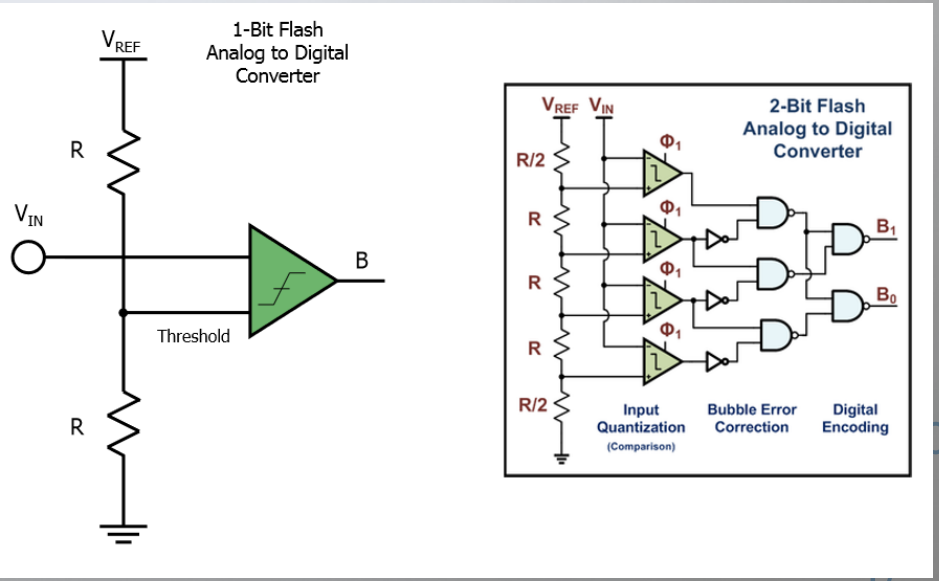
- Energy measurement (Scintillator+PMT)





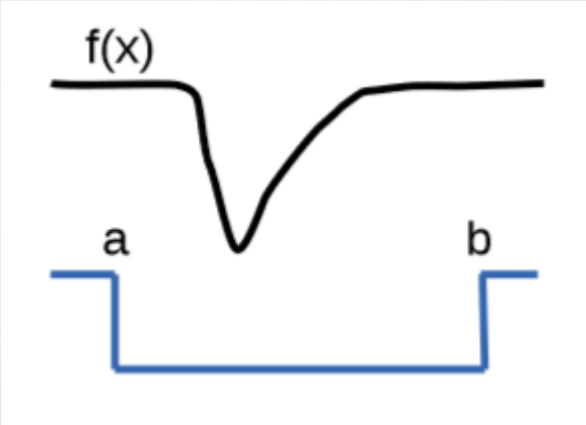
ADC

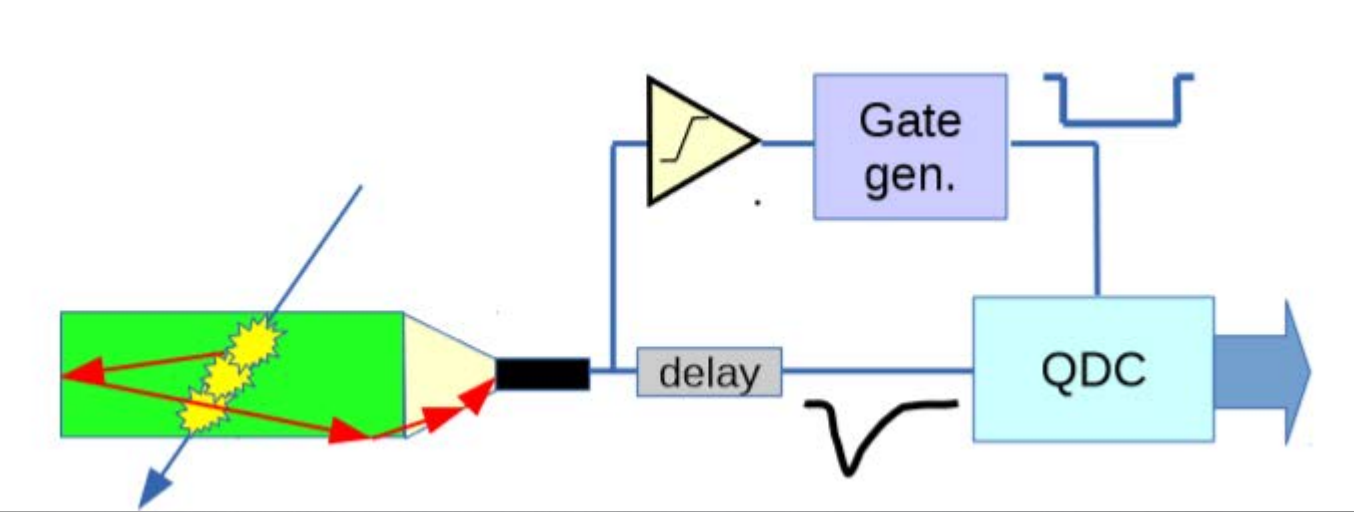
- Analog to Digital Converter
- Oscilloscope, Digital audio encoding…
- Resolution, Sampling Rate, Range
- Flash, Successive approximation, Pipeline
- Charge ADCs (QDC)
- Peak sensing ADC



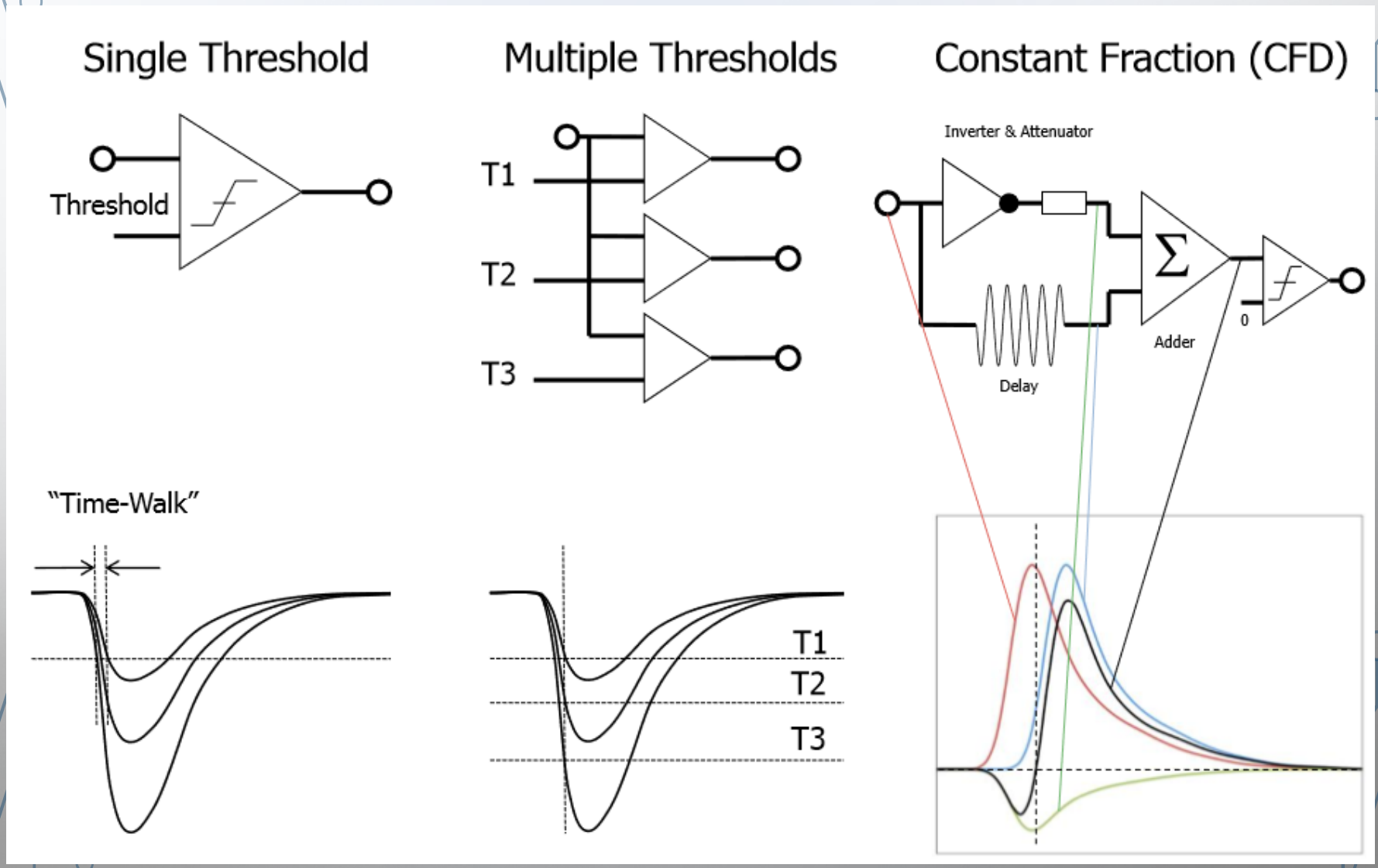
QDC

- Charge to Digital Converter
- Integrator+ADC
- Pedestal subtraction

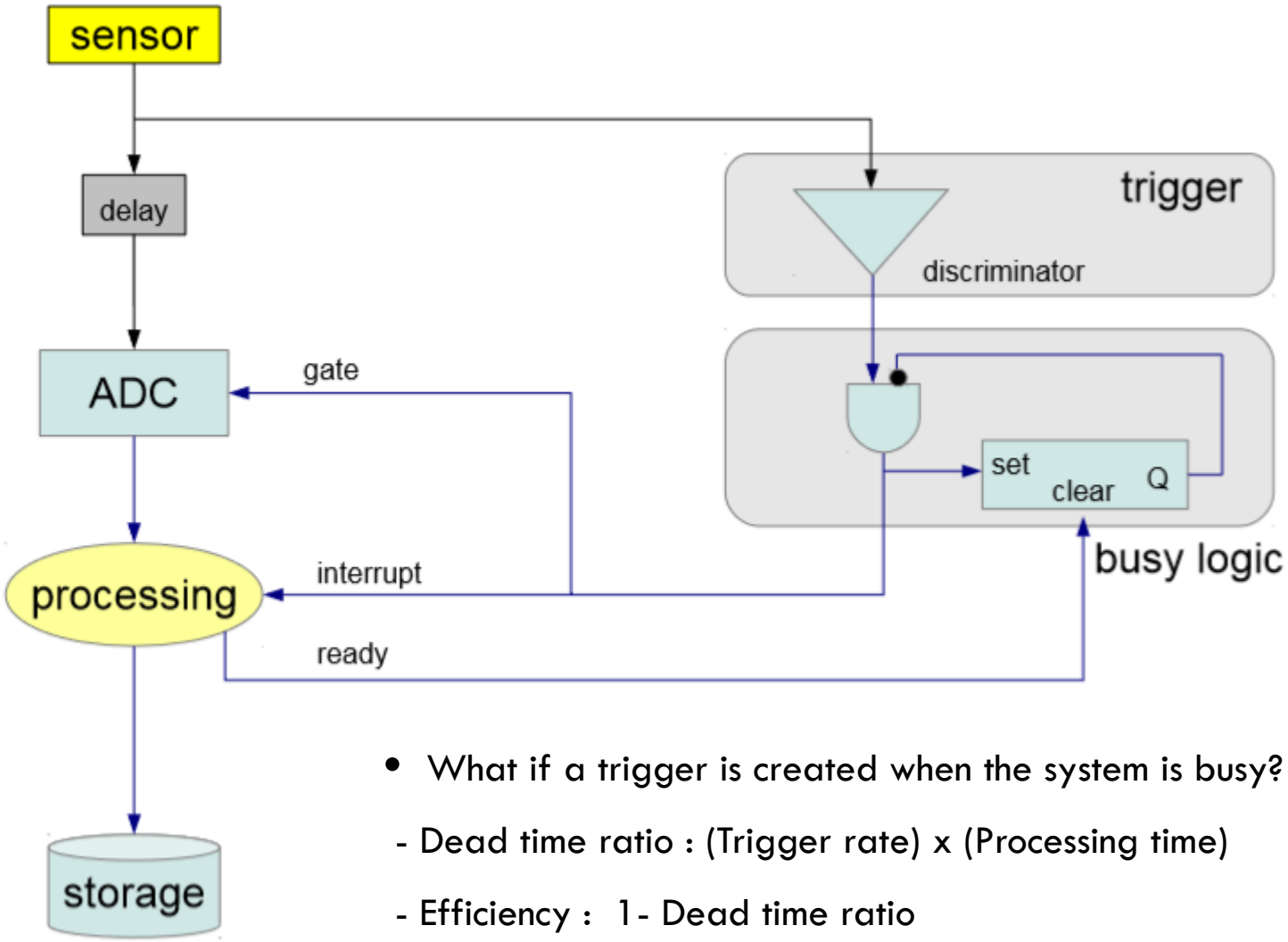




DISCRIMINATOR



SIMPLE EXAMPLE – BUSY LOGIC

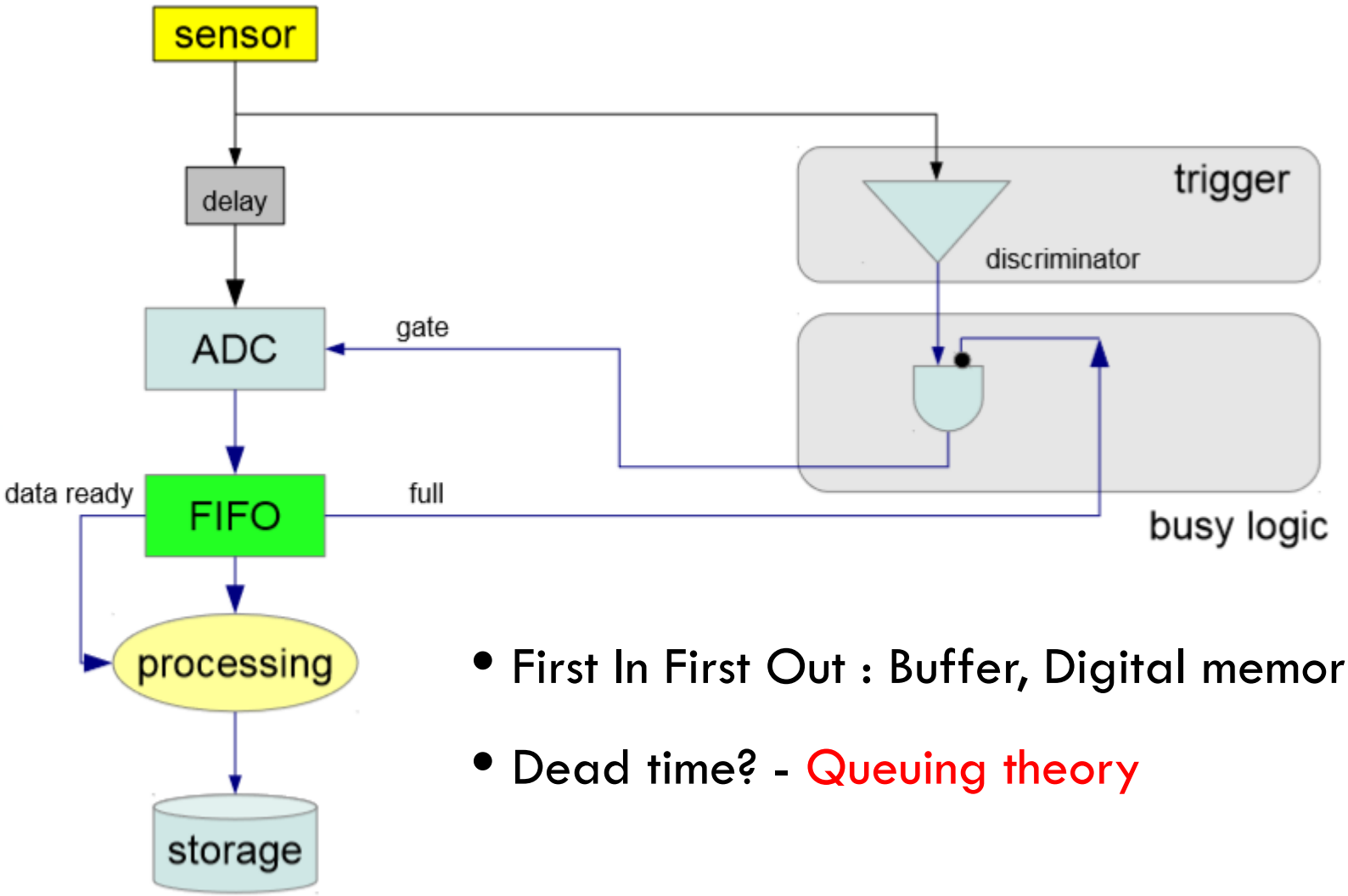


- What if a trigger is created when the system is busy?

- Dead time ratio : (Trigger rate) x (Processing time)

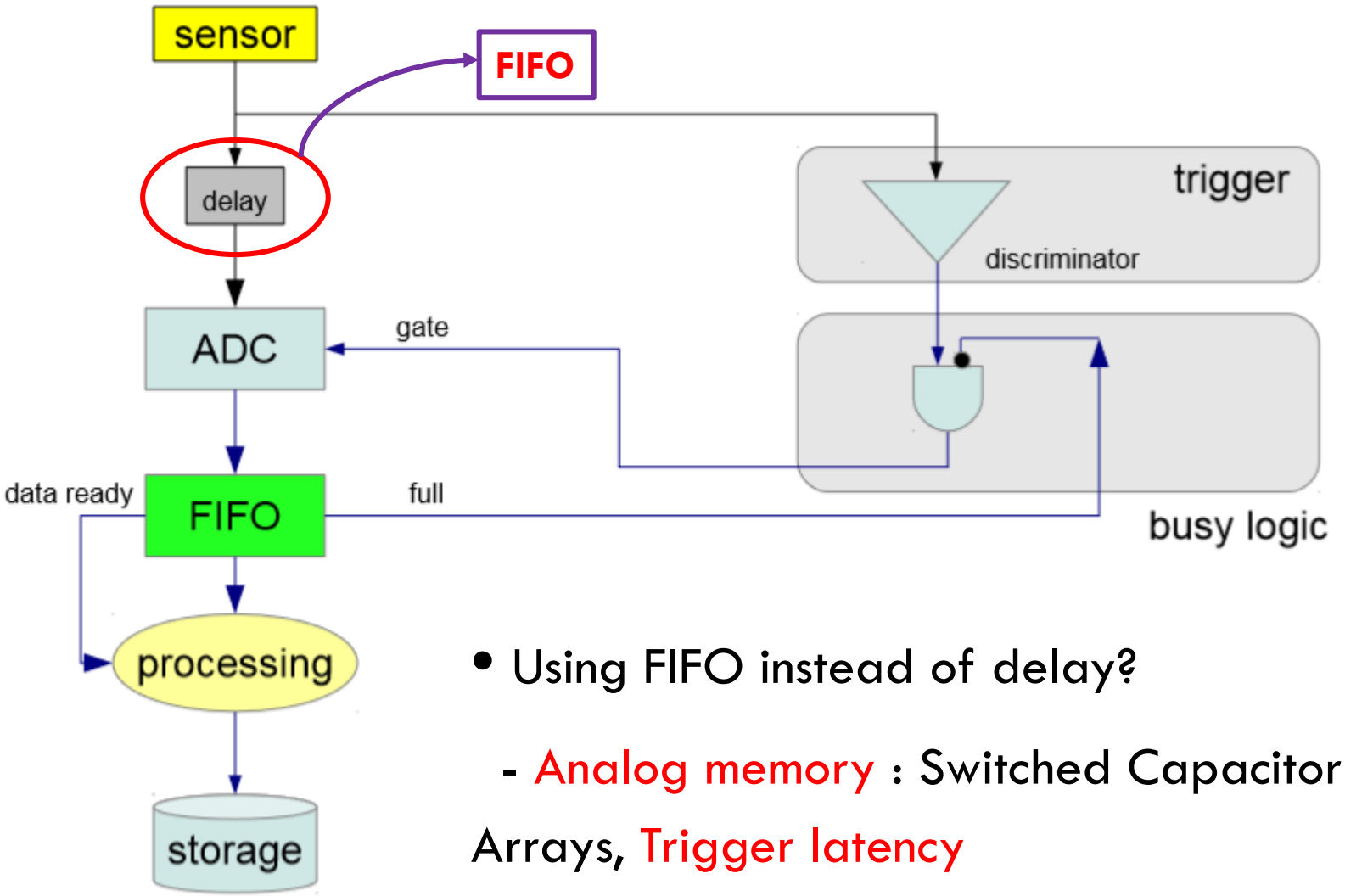
- Efficiency : 1- Dead time ratio

SIMPLE EXAMPLE – BUSY LOGIC



- First In First Out : Buffer, Digital memory
- Dead time? - Queuing theory

SIMPLE EXAMPLE – BUSY LOGIC



- Using FIFO instead of delay?

  - Analog memory : Switched Capacitor Arrays, Trigger latency

WHAT ELSE? - TDC

- Time to Digital Converter
- Digital counters

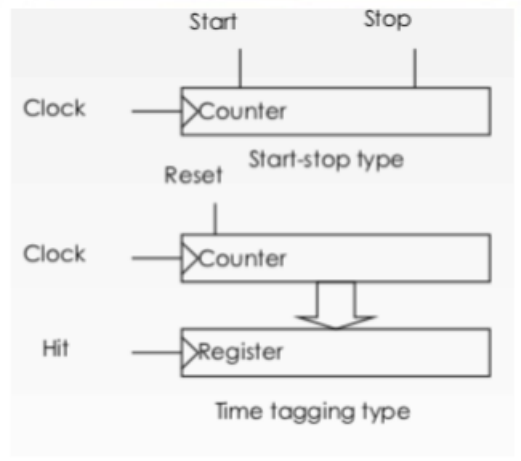
  - Good and cheap time references available as crystal oscillators

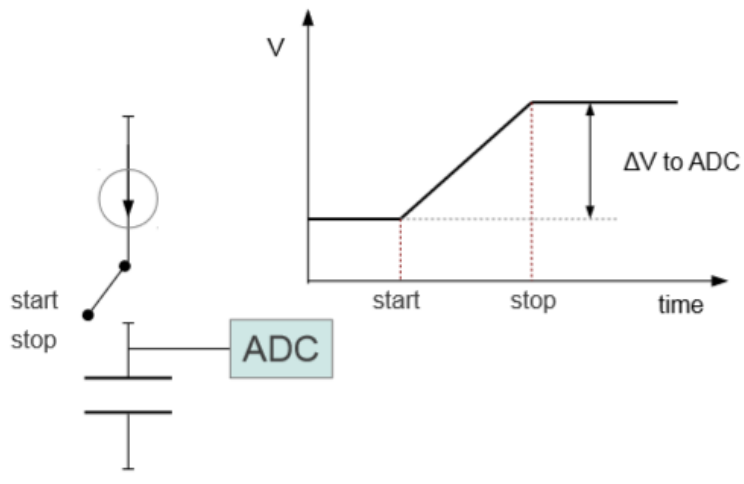
  - Limited resolution: ~1ns

- Charge integration (start-stop)

  - Limited dynamic range

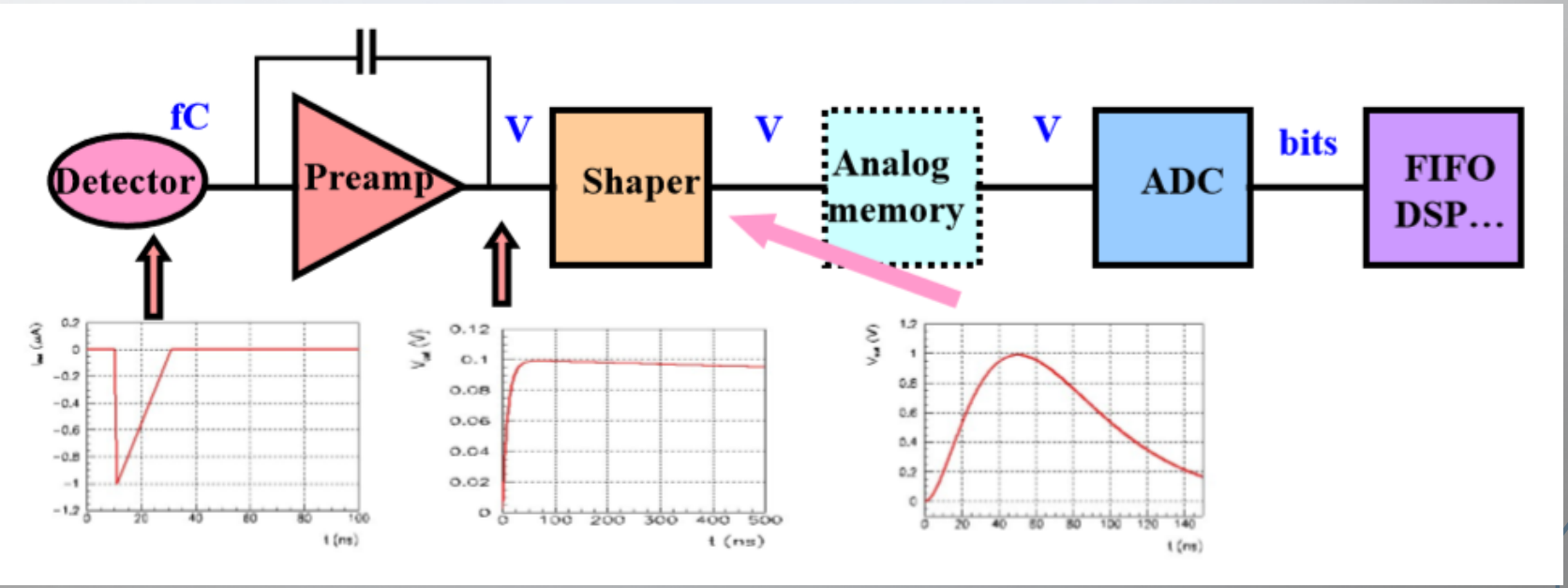
  - High resolution: ~1-100 ps





WHAT ELSE? – PREAMP, SHAPER

- Charge sensitive preamp
- Pulse shaper



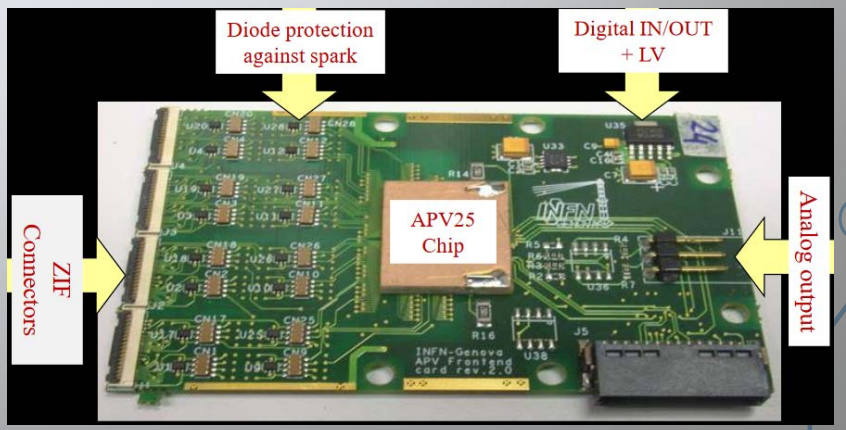
THE FRONT END ELECTRONICS

- Electronics directly connected to the detector (sensitive element)
- Acquire an electrical signal from the detector (usually a short, small current pulse)
- Tailor the response of the system to optimize
  - the minimum detectable signal
  - energy measurement (charge deposit)
  - event rate
  - time of arrival
  - insensitivity to sensor pulse shape
- Digitize the signal and store it for further treatment

SCALING UP - ADDING MORE CHANNELS

Single or few channels

ASIC

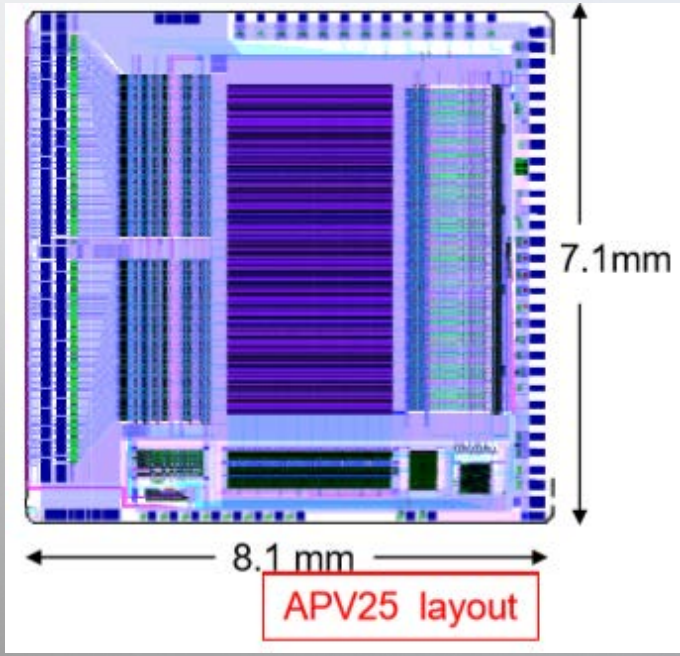


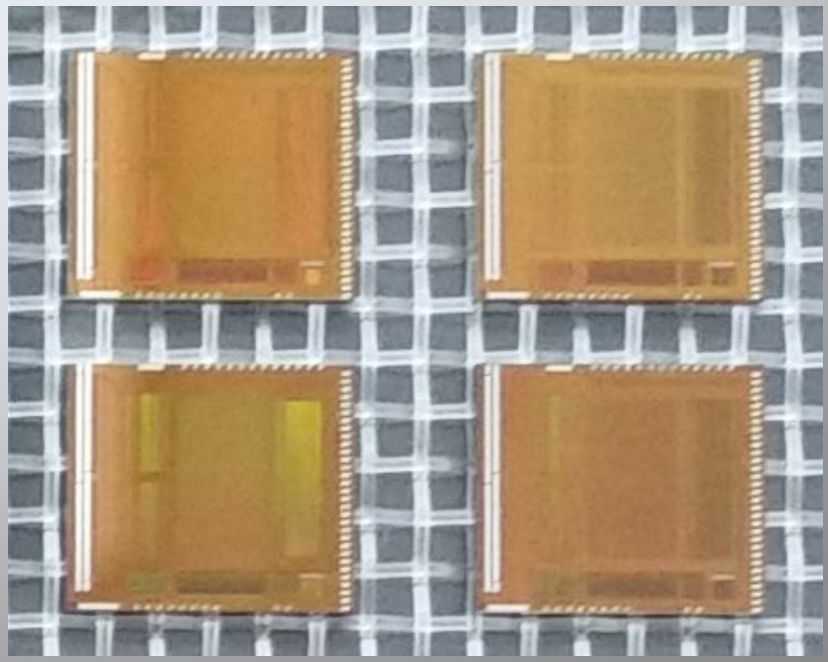
~ 10s, ~100s channels

ASIC

- Application Specific Integrated Circuit

  주문형반도체





(SEMI?) ASIC

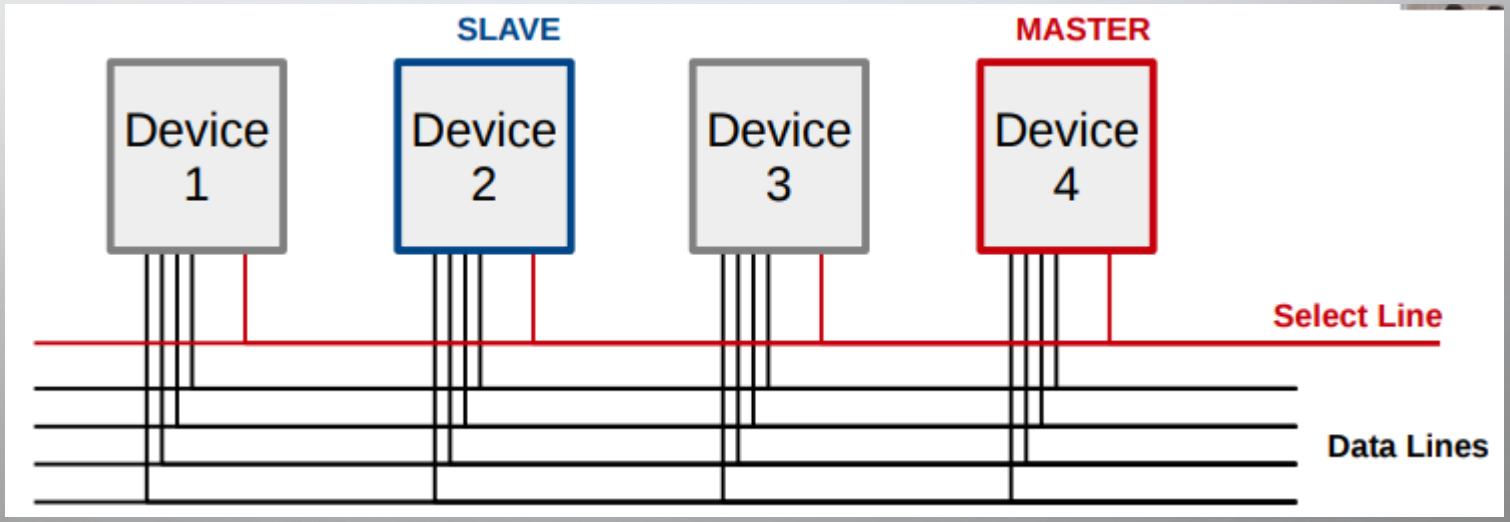
- Weeroc : Special ASICs for particle detector applications

	SiPM	MA-PMT	PMT	APD	Pin diode	Silicon strips	RPCs	Micromegas GEMS
Maroc 3A	×	✓	✓					
Catiroc 1	×	×	✓					
Spaciroc 3	×	✓	✓					
Citiroc 1A	✓							
Petiroc 2A	✓						×	
Photoroc 1A	×	✓	✓					
Triroc 1A	✓							
Skiroc 2A				✓	✓	✓		
Hardroc 3B	×	×					✓	
Gemroc 1				×	×	×		✓

✓ Optimized for - × Compatibility - × Compatibility (not tested)

COMMUNICATION - BUS

- A bus connects two or more devices and allows the to communicate
- The bus is shared between all devices on the bus → arbitration is required
- Devices can be masters or slaves (some can be both)
- Devices can be uniquely identified ("addressed") on the bus



COMMUNICATION - BUS

- Famous examples: PCI, USB, VME, SCSI
  - older standards: CAMAC, ISA
  - upcoming: ATCA
  - many more: FireWire, I2C, Profibus, etc…
- Buses can be
  - local: PCI
  - external peripherals: USB
  - in crates: VME, compactPCI, ATCA
  - long distance: CAN, Profibus
- Theoretically ~ 16 MB/s can be achieved
- Better performance by using block-transfers
- Easy to add new device, boards with standard interface

COMMUNICATION - NETWORK

- All devices are equal

  - Devices communicate directly with each other via messages

  - No arbitration, simultaneous communications

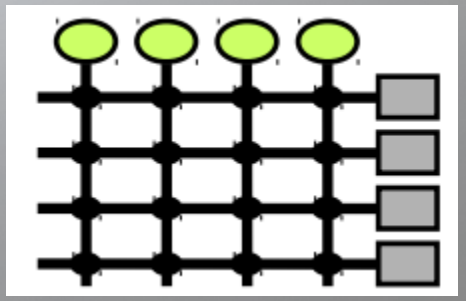
- Examples: – Telephone, Ethernet, Infiniband, …

- In switched networks, switches move messages between sources and destinations

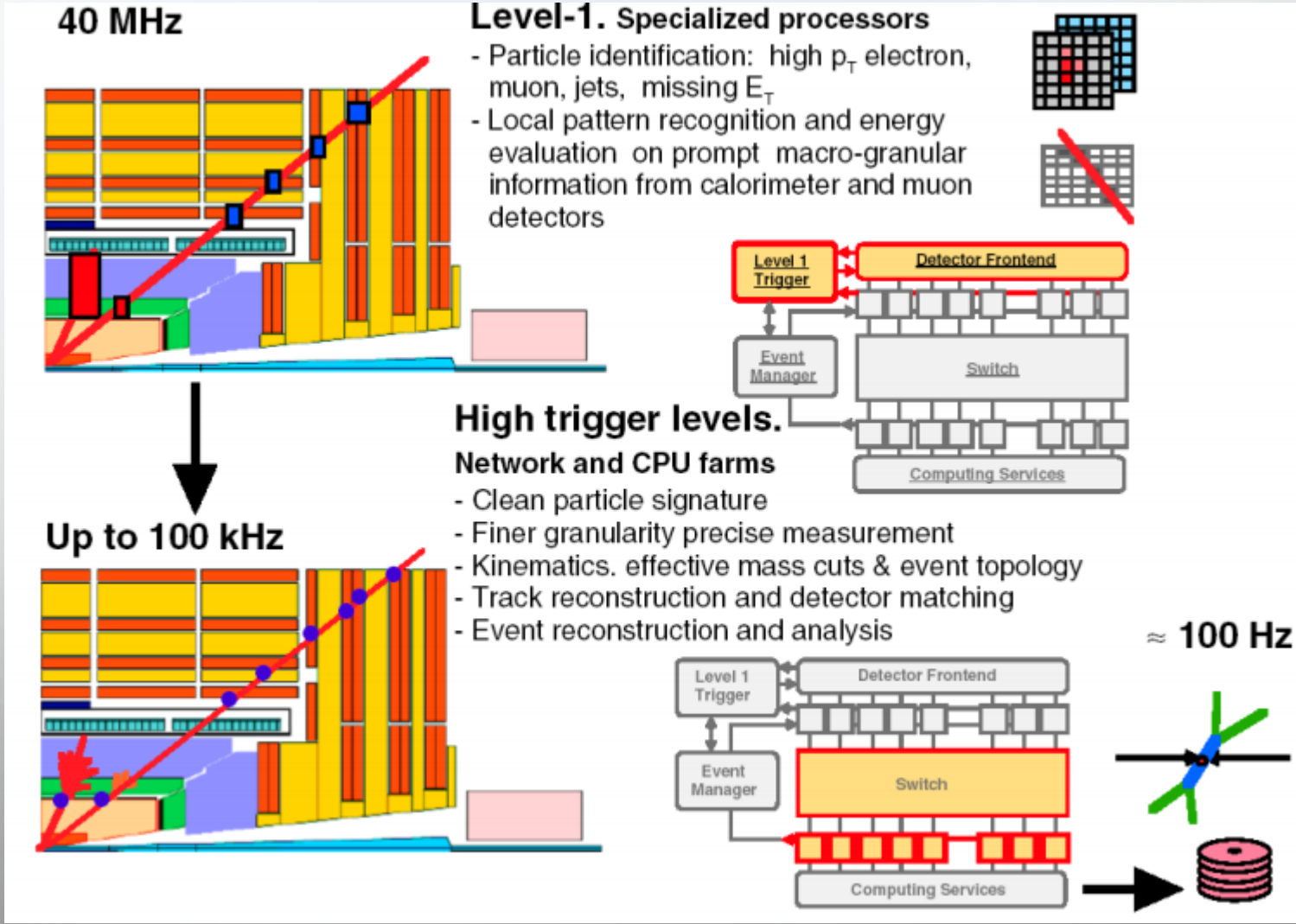
  - Find the right path

  - Handle congestions (two messages with the same destination at the same time)

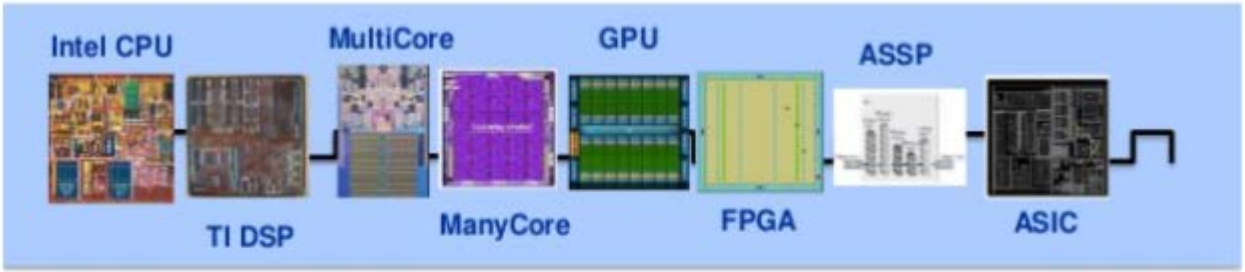
  - The key is …. buffering



MULTI LEVEL TRIGGER - CMS



ASIC, FPGA, GPU, CPU



Flexibility, Programming Abstraction

Performance, Area and Power Efficiency

CPU:
- Market-agnostic
- Accessible to many programmers (C++)
- Flexible, portable

FPGA:
- Somewhat Restricted Market
- Harder to Program (Verilog)
- More efficient than SW
- More expensive than ASIC

ASIC
- Market-specific
- Fewer programmers
- Rigid, less programmable
- Hard to build (physical)

	ASIC	FPGA	GPU	CPU
Front-end	✔	(✔)		
L1	✔	✔	?	
HLT			(✔)	✔
Offline/Grid		$	$	✔

FPGA

- FPGAs have been around in trigger systems for a while
- Latest large FPGAs give a huge amount of flexibility and are used in the LHC experiments
- Easily upgrade trigger systems since the logic (algorithms) do not need to be fixed when the board is produced
- Can change the algorithms running in hardware, in light of better detector understanding, even physics discoveries
- Deep learning?

인공지능 칩 강자는 누구? GPU vs FPGA vs ASIC (1)

딥러닝 빠른 연산처리와 데이터센터 에너지 효율, 하드웨어가 '핵심'

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